JonJu Tech Ltd.

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WP type: Engineering **Date**: 5th February 2021

Title: Electromagnetic Compatibility (EMC)

Contents

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Lecture Plan for Product Design Induction

Duration: 50 mins Date: 27th April 2022

Number of students: unknown but could be anywhere between 5 and 40.

General equipment: whiteboard with markers and eraser (deliverer); writing materials, web access for lecture – at front and visible to everyone. Don't rush with this.

1. Plan

Task	Obj ref	Action	Equipment	Time (mins)
Introduction: my credentials;	-	Verbal.		2
Lecture on EMC		Introduce – snapshot – rules of thumb vs. Maxwell. Deliver verbally Journey of rules of thumb.	Screen/Whiteboard	3
Grounding		Page 4 of EMC doc. Everything has impedance, and in EMC inductance most important – ground plane/common paths/Z tend to 0.	Screen/Whiteboard	3
Magnetic Induction		Page 4 EMC. Explain – formula – issues. Relate to PCB circuit. Tracks on PCB	Screen/Whiteboard	5
Electric Induction		Page 5 EMC. Gen circuit/formula/issues/relate to PCB (watch XTAL)	Screen/Whiteboard	5
General Coupling comments		P 6 EMC. Just go through the points	Screen/Whiteboard	3
High frequency		P. 7 EMC doc. Form, dimensions, and material – Zo, etc.	Screen/Whiteboard	3
Near and far fields		P. 7 EMC doc. Stick with far – $d=\lambda/2\pi$ rough transition point	Screen/Whiteboard	3
Coupling Modes		Page 8 EMC Doc. Common mode dominant in EMC – usually where the problem is. Go through modes showing how current flows.	Screen/Whiteboard	5
3 examples		Page 11 EMC doc. Go through 3 examples	Screen/Whiteboard	5
Questions		Whatever	Screen/Whiteboard	5
Sell JJT		Pitch for placements	Business cards	3
			Total	**45**

What it is all about

Electronic products interfere with each other via radio waves. A given product may emit unacceptable levels of radio interference and interfere with other products, or the same product may have been designed such that it is unacceptably sensitive to radio transmissions and suffers in performance as a result. This phenomenon is EMC. Such limitations are combatted by regulations (CE marking, FCC), testing (formal testing of products at approved test houses), and the following of good design practice. This White Paper covers this topic.

Quick Learn

- EMC is all about making sure a product neither interferes with others, or others do not interfere with it (with radio waves)
- Good design practice improves the likelihood a given product will be compatible, but only testing can verify it. A designer cannot be asked to 'design in' EMC compliance.
- Risk assessment and testing (depending on the exact standards required) are the two means by which EMC is confirmed, but the latter is the only one recommended by JonJu Tech Ltd.
- Not all products have to meet the same standards. There are specific standards for specific product types.
- Do not attempt to gain approval levels above those required – increases cost and risk and delivers no benefit.
- Find a good a test house that will guide you through this process (Product Approvals www.productapprovals.co.uk)
- Do not abandon the process and leave it to the test house. Make sure you understand what is being done, possible outcomes and risks.
- Budget on about £1,000/day and between 3 and 5 days of testing.
- Accept that the design may need to be changed and more prototypes built.

Key Actions/Advice

As Quick Learn

Rigour

When an electronic device is designed, it may fail to function in the presence of electromagnetic noise from other systems or cause other electronic devices to malfunction because of its radiated or conducted emissions (**EMC failure**).

Electromagnetic noise is classified as being either **conducted** or **radiated**, the former being noise that is conducted along elements of the design, cables, PCB tracks, etc., and the latter noise associated with electromagnetic waves propagated through the atmosphere. Note that conducted noise and radiated noise are bi-directional, i.e. noise created by the equipment under test [EUT] **(emissions)** can contaminate systems outside it with either type of noise, and it can also receive and be disrupted **(immunity)** by noise of these types.

The laws by which electromagnetic waves couple with objects in space are extremely complicated: especially when the systems being modelled are not the regular shaped approximations found in textbooks (Maxwell's equations mathematically define and solve such problems), but solving real EMC issues depends far more on having the right rules of thumb, approximations, experience and simple circuit models available in one's head. If complex calculations are considered necessary, there are software packages available (https://www.ansys.com/).

It is possible to go to inordinate lengths to limit the adverse effects associated with EMC, but, as is the case with all engineering, performance must be traded against the cost and time necessary to implement the said precautions. Only experience and diligence can be used to do this, but the issue is briefly raised here to make the reader aware of it.

The information in sections 2.1 to 2.11 is sufficient to allow the reader to understand almost any practical EMC problem and its resolution. Section 2.12, *Examples of EMC issues and suggested solutions for the same*, is very far from exhaustive: more examples can be found in Tim Williams (see references), and it is also recommended that the reader adds his own examples to 2.12 as experience allows.

1Interference coupling mechanisms

Whatever the application, an analysis will involve a system of **sources**, **victims,** and **coupling** between the two. The coupling can be via a **direct conductive connection**, such as a cable, by **magnetic induction**, **electric induction**, or by a combination of any or all of the foregoing.

It can be useful to create a block diagram of a system and to identify on it sources, victims and coupling mechanisms. This allows for a systematic approach to problem solving, but it is also worth noting that such diagrams can evolve, e.g. a PCBA will be a system in itself; creating ground maps can also be a useful exercise.

Conductive Connection

As the title suggests, this type of coupling is a physical connection between source and victim, and this link might be a PCB track, component or cable. The first thing that must be emphasized is that **when dealing with EMC everything has impedance**. A copper track on a PCB and a cabled connection has resistance and inductance.

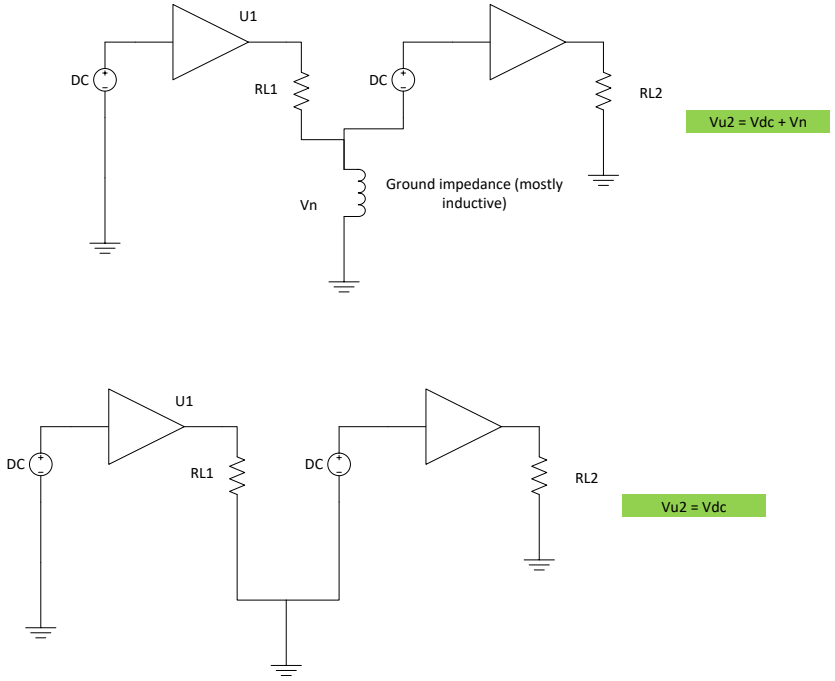


Fig 1

KEY POINTS:

- ***Ensure that the physical value of impedance is minimised in cases where connections would ideally have Z=0, e.g. the ground impedance in the first circuit above – use a plane instead of tracks for ground.***
- ***Make sure that common return paths for currents are avoided to a maximum degree. The issue is that a noise voltage can develop at a victim simply because two elements share the same ground impedance. This is illustrated in the circuits of Fig 1 and could be caused by a common ground track for both amplifiers in the first circuit, as opposed to both amplifiers connecting to the same ground point at the entry to the PCBA in question, as is the case for the second circuit.***

Magnetic Induction (coupling between inductive loops)

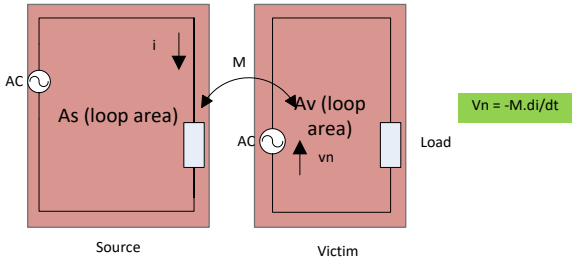


Fig 2

The area of the loop defined by the source (As), the rate of change of current (di/dt), and the area defined by the loop of the victim (Av), couple to induce a noise voltage (vn) in the circuit of the victim.

A way to reduce the effect described in the previous paragraph would be to introduce of a ground plane instead of using tracks to implement ground, because the loop area is then limited to the thickness between the ground plane layer and the track in question (thickness of just one layer of the PCB, ideally), rather than having the large circuitous route that might be the case with a tracked ground.

The magnetic induction noise voltage in equation 2.3.1 gives all the pointers necessary for the minimisation of magnetically induced noise. Note that this noise voltage (Vn) is independent of source or load impedances in the victim.

$$Vn = -M.di/dt \qquad 2.3.1$$

KEY POINTS:

- ***To minimise M, the mutual inductance, reduce the loop areas of both the source (As) and victim (Av)-see figure 2.***
- ***Increase the separation between the source and victim's loops to further reduce M***
- ***Consider reducing the switching frequency in the source***
- ***Consider band limiting the switching waveform to reduce the maximum di/dt***

Electric Induction (coupling between voltage nodes)

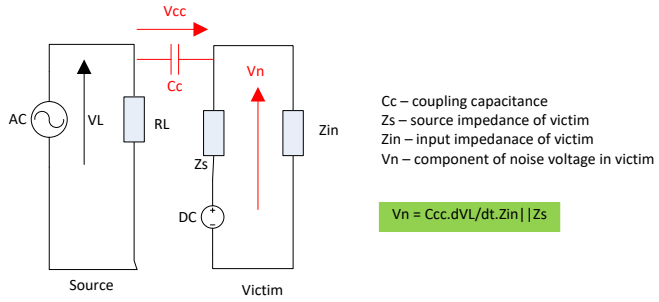


Fig 3

Electric induction involves a capacitive coupling (Cc) between two voltage nodes on the victim and source. This mechanism acts as a current source in the victim (current squirter).

The noise voltage (Vn) present in the victim is derived as follows:

$$Vn = icc.Zvictim \qquad 2.4.1$$

The impedance seen by the noise current (icc) is the parallel combination of source and load in the victim (by Thevenin); and the voltage switched across Cc is VL under the assumption that Xcc >> Zin||Zs (proportion of VL dropped across Cc is much greater than Vn, and therefore approximates to VL).

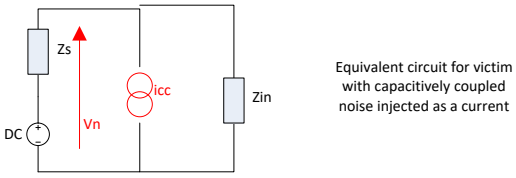


Fig 4

Using the equivalent circuit of the victim, Fig 4, and noting that the current in a capacitor is its value times the rate of change of voltage across it, the noise voltage (Vn) will become by substitution into 2.4.1:

$$Vn = Cc.dVL/dt.\ Zin||Zs \qquad 2.4.2$$

Using this formula it is possible to make some key observations.

KEY POINTS

- ***Reduce Cc by: shielding between source and victim; increasing the separation between source and victim; reducing the surface area of the conducting nodes that form Cc (metallic surface area)***
- ***Reduce the dVL/dt in the source, or band limit it to reduce harmonics***
- ***Assuming Zin>>Zs, which is likely to be the case, reduce Zs (note impedances are in parallel)***

General comments on coupling

A useful deduction, evident from equations 2.3.1 and 2.4.2, is that magnetic induction is independent of the impedances (Zs, Zin) in the victim, but electric induction is dependent on both of them.

KEY POINTS

- ***Vary the input impedance, Zin or Zs, of the victim's circuit to determine if noise is from magnetic or electric induction (if magnetic the noise will not change, if electric, it will.)***
- ***All of the above techniques for modelling EMC issues are conditional on the system in question being of low frequency (length of circuit < λ/4). High frequency models are covered later in this document.***
- ***Cables couple with electromagnetic noise most effectively when the frequency in question is at the same frequency as the frequency of resonance of the cable (approx. 30MHz).***

Near End and Far End Crosstalk (NEXT, FEXT)

Deriving formulas for near and far end crosstalk using the theory developed in the previous sections is fairly straightforward (see section 10.2.1.1 – Tim Williams), but perhaps not entirely necessary since the principles for reducing crosstalk are simply the reduction of magnetic and electric induction, as described above. There are some observations that may help to identify the source of noise (see Key Points).

KEY POINTS

- ***Note that the analysis in this section is on the basis that circuit length is less than λ/4. If it is greater the high frequency section below applies.***
- ***If FEXT and NEXT are approximately the same but inverted in relation to each other, then it is likely that coupling is predominantly magnetic. If they are the same and in phase it is likely the dominant coupling mechanism is electric induction.***
- ***All the rules for reducing magnetic and electric induction apply to crosstalk too.***

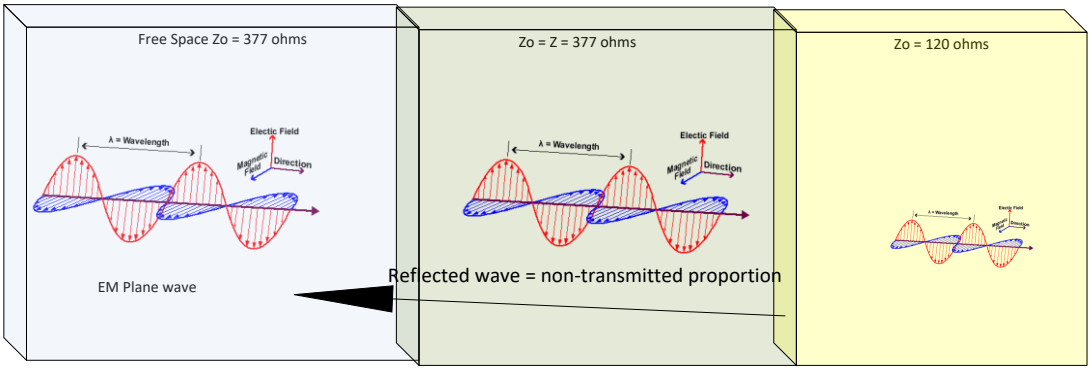
High Frequency Model

At high frequencies (length of circuit >λ/4) magnetic and capacitive coupling cannot be modelled with single 'lumped' components, because under high frequency conditions there are an infinite number of capacitive and magnetic coupling components that are interdependent. In order to cope with this, it is necessary to leave the restrictive approximations of circuit theory and enter the domain of field theory (Maxwell's equations), but it is still not necessary to study the complex mathematics underpinning field theory because a few explanations and rules of thumb will allow high frequency systems to be designed and adequately (usually) modelled – certainly as far as most PCBA designs are concerned.

Getting to grips with designing PCBAs with good electromagnetic compatibility requires an understanding of the following concepts:

Characteristic impedance and impedance matching

This document assumes the reader has knowledge of transmission lines and basic field theory. Characteristic impedance (Zo) is a property that all high frequency transmission media have, and, if matched and physically connected, i.e. two different media have the same characteristic impedance, then an electromagnetic wave in the first will entirely pass into the second without reflection. Furthermore, if the transmission media have different Zo then only a proportion of the wave will be transmitted and the balance reflected, the limiting cases being total reflection for a line terminated in an impedance of Zo = ∞ or Zo = 0. These properties are essentially frequency independent, providing the circuit length > λ/4. The principles above apply to propagation over free space and propagation over man made media such as coaxial cables, PCB striplines, etc. The diagram below illustrates this.



The characteristic impedance of man-made transmission lines, such as PCB stripline or coaxial cables, and assuming lossless lines, are determined by the geometry and dimensions of conductors, insulators and the properties of the materials – principally the insulation permittivity. Calculation and/or measurement of such values are beyond the scope of this report.

Near and far fields

The EM waves in the section above are known as plane waves (E field [red] is perpendicular to the H field [blue]). These exist in free space and correspond with Zo = 377 ohms, which is all fine as long as the analysis is taking place in what's known as the **far field.** The far field is the propagation space at an appreciable distance from the source of the EM wave, at which distance, all other things being equal, electromagnetic waves will be plane. The **near field** has different properties that are not easy to predict and result in wave impedances that can be anywhere between about 30 and 3000 ohms, which means unexpected reflection and transmission may result.

It really is very difficult, and likely pointless, to try and predict exactly what is going on in the near field. Most near field effects are caused by **common mode** noise, which is covered in the following section: it is simply necessary to take all possible steps to reduce common mode noise.

KEY POINTS:

1. ***According to Maxwell's equations the transition from near field to far field occurs at λ/2∏. This gives the designer a guide upon which to estimate whether whatever conclusions he is coming to apply to the near or far field.***
2. ***Note that cables magnetically couple at lower frequencies (<30MHz) and are most receptive to coupling at frequencies at which the cable resonates.***

Coupling modes (differential, common and antenna modes)

It is very important that engineers thoroughly grasp the notions of common, differential and antenna mode noise coupling – common mode noise is particularly important when considered with respect to EMC. This section is all about magnetically induced currents – suggest re-read of section 2.3 before assimilating that which is immediately below.

Differential Mode Noise

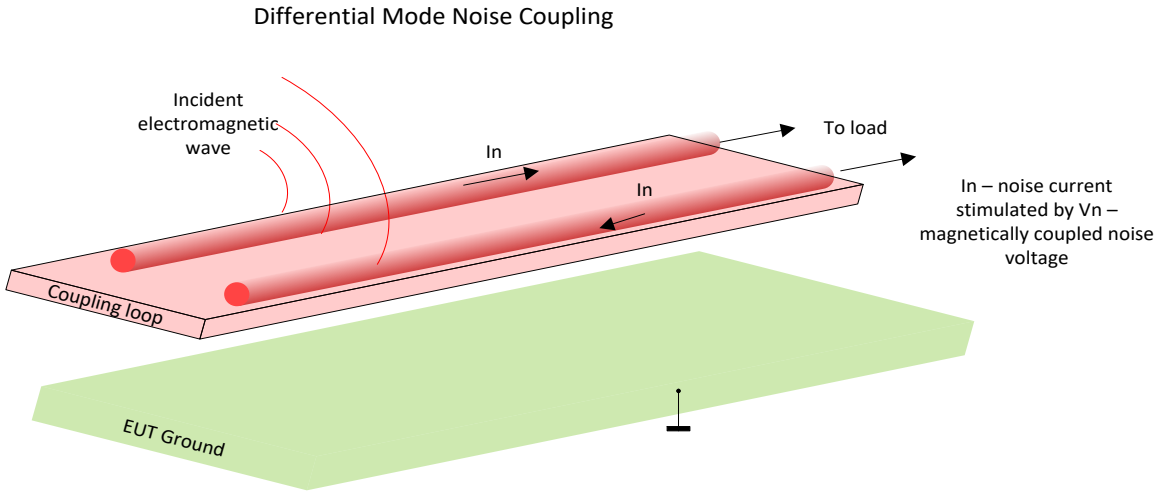


Fig 5

Differential mode noise is the current induced by an electromagnetic wave that couples with the signal/power circuitry (cable in Fig 5) **only.** This creates a noise current in the loop according to the principle explained in section 2.1.3 (magnetic coupling), and this current will flow around the loop, thus making it have a 'go' and 'return' path, but this path is not necessarily in sympathy with the direction of any signal current flowing in these cables.

Common Mode Noise

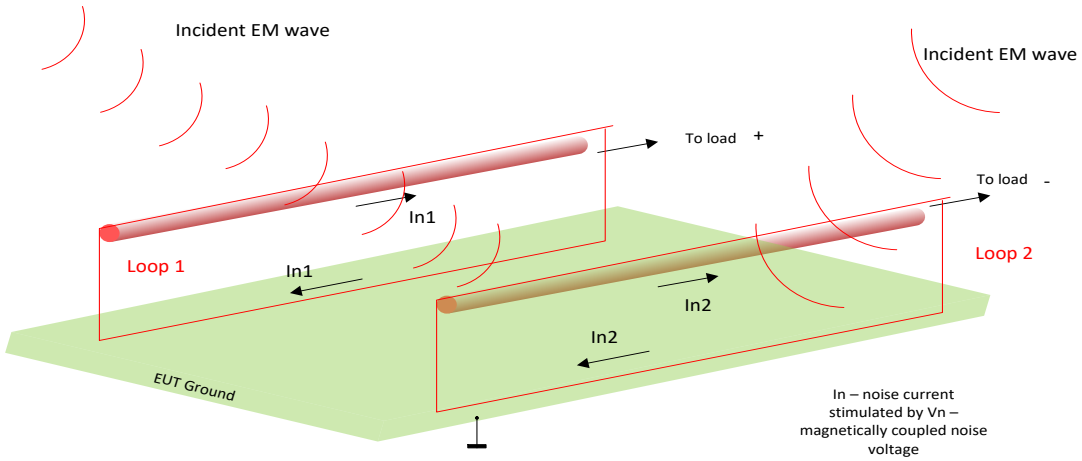


Fig 6

Common mode noise is generated when an external magnetic field couples with the loop set up by ground and each signal/power carrier (cable in Fig 6) independently, which results in currents in the cables that flow in opposition to each other: but these should not be thought of as currents that are on a collision course with each other in the load - the coupling is relative to ground rather than through the load. It is a mistake to think of common mode currents flowing in opposition through the load, they aren't. They are flowing in a loop relative to ground. Also note that two EM waves have been drawn, but it may be the same EM wave that couples with both loops.

Antenna Mode Noise

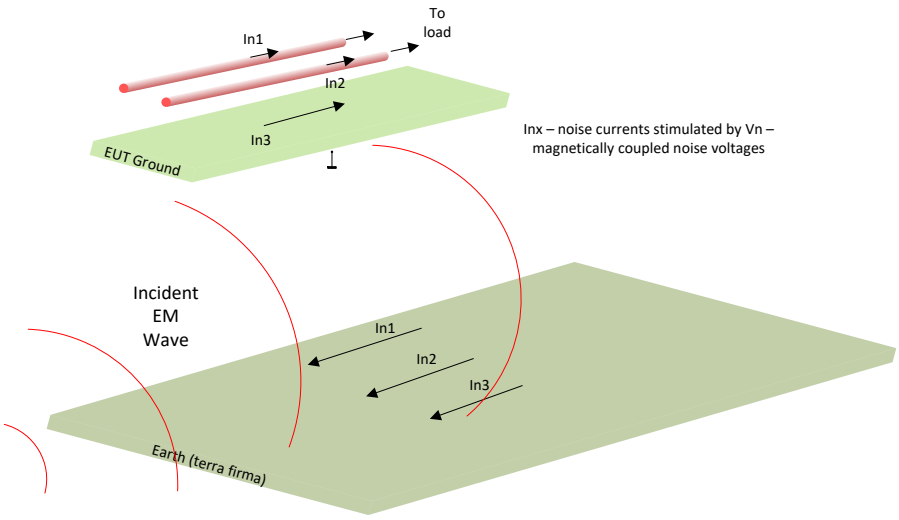


Fig 7

Antenna mode is similar to common mode in that currents flow relative to ground reference, but that reference is the ultimate ground reference –terra firma. The incident EM wave couples with loops set up by the EUT and terra firma, in this case 3 loops inducing currents In1, In2, In3. The principle is the same as the common mode case except the low side reference is terra firma (Earth) instead of the EUT ground.

KEY POINTS:

- ***Common mode noise is the dominant issue in most cases when considering EMC***
- ***Don't become confused by signal currents, they are essentially independent of these mechanisms, although there is a mechanism by which common mode noise can be converted into differential mode noise (see section 2.12)***

Mains Electricity

The main things to consider when assessing mains supply to a product that is to be EMC assessed are: the quality of the mains supply in the first place which, although variable, is outside the control of the electronics engineer; the propensity for the mains to become contaminated with common mode noise from the EUT (conducted emissions); and the ability of the EMC filtering and power supply design to reject noise such that it doesn't appear at the input of the EUT (equipment under test).

It is recommended that fully approved, commercial PSUs (the choice may be a function of the EN standards that are to be tested against) are used with differential and common mode filtering on the mains input to the EUT.

If the reader wishes to delve into issues with the mains supply Tim Williams (in references) covers them admirably.

KEY POINTS:

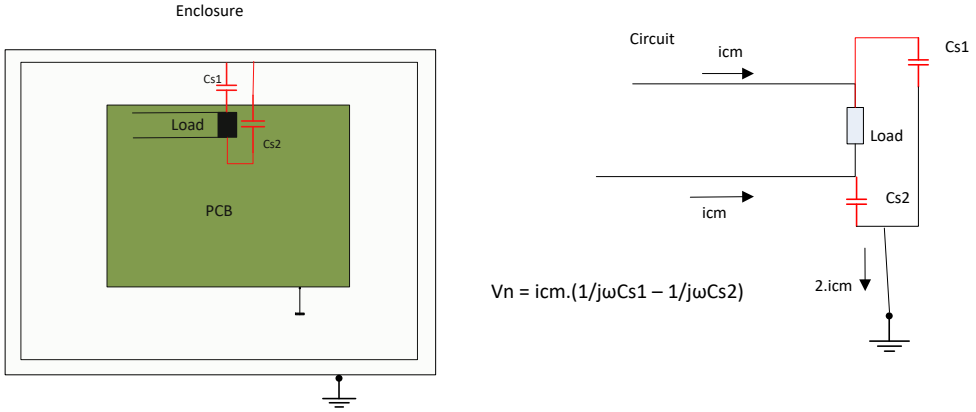
- ***Use commercial EMC/EMI mains noise suppression products, or discrete component filters, if such are needed for the product. These assist with passing conducted emissions and immunity tests.***
- ***Use fully approved power supplies from reputable suppliers, and the model of supply chosen may be determined by the EMC standard it is necessary to pass.***
- ***Note that whilst the PSU supplier has a responsibility to provide a product that will reject noise it sees at its input, it doesn't have a responsibility to reject noise that an EUT might push back onto the supply (impossible to do this because the PSU designer can't know the details of loads that might be applied). The CMRR (common mode rejection ratio) should not be considered as reciprocal. The upshot of this is that the PSU should not be considered as a panacea for rejecting conducted noise emanating from the EUT – the product designer must take responsibility for it.***
- ***Use transzorbs and other protection and clamping systems to protect the design from unexpectedly high voltages (surge tests that simulate lightning strikes on cables are done as part of standard EMC testing), over and above the filtering offered by the commercial EMC filter.***
- ***Design firmware such that it will always reset and recover after noise that could cause a microprocessor failure has ceased(watchdog timers (external better – but use both software and hardware WDTs if appropriate), write hardened firmware, etc.).***
- ***Consider the use of ferrites both in the design of the product and in the external cabling to suppress noise, if necessary (note external ferrites are often the means by which a product is nudged into a condition that permits a pass).***
- ***Note that inductors have most effect at lower frequencies and ferrites higher ones.***

Examples of EMC issues and suggested solutions for the same

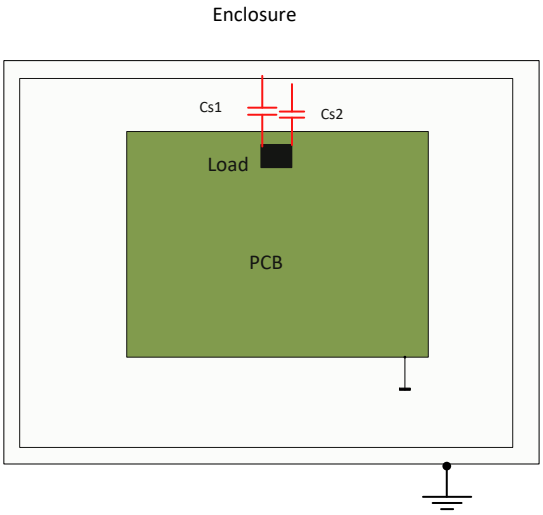
There are a multitude of noise scenarios and it isn't practical to list them all and explain how using the theory above can overcome them, but it is possible to use the methods to work out solutions for a very wide range of issues. There are a few examples below which should help to illustrate this.

There is no substitute for experience so the advice of this report is to grasp every opportunity possible to work on products needing EMC approval. With the foregoing theory it will usually be possible to work out the cause of noise and find ways to minimise it.

Example 1 – Common Mode Noise causing Differential Mode Noise



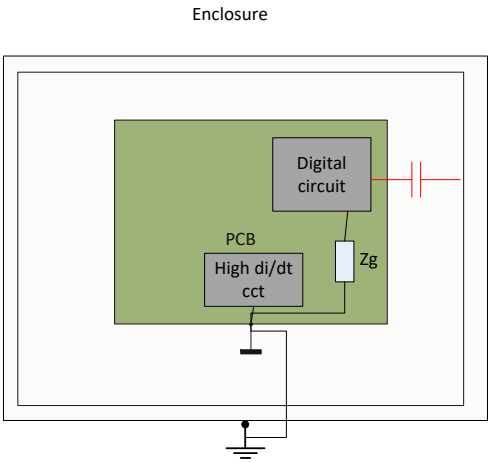
Stray capacitance between each end of a load and the case can cause common mode currents (icm) to generate differential mode noise (vn) across a load as above: because Cs1 ≠ Cs2. This can be improved by physically turning the load through 90 degrees as in the diagram below (result is Cs1 = Cs2).

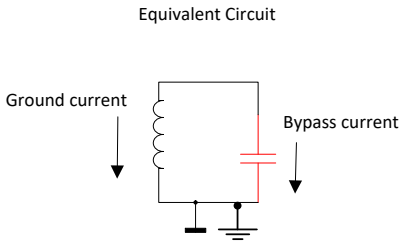


$V_n = i_{cm}.(1/j\omega C_{s1} - 1/j\omega C_{s2})$
$V_n = 0$ if $C_{s1} = C_{s2}$

Example 2 – Using Casing Capacitors to Circumvent high Ground Impedance on a PCB

Ground paths, tracks and planes on a PCB have inductance. At high frequencies the resulting impedance can be such as to introduce unacceptable differences in the ground potentials at various points around a PCB. Ground inductance is usually of the order of tens of nanohenries, so noise in a 20nH ground carrying 100µA might result in a noise voltage of 62µV at a frequency of 5MHz ($V_n = \omega L.i$). It becomes necessary to find ways of reducing the effective ground impedance when noise voltages generated in this fashion are unacceptable, and this is often done as shown in the diagram below.

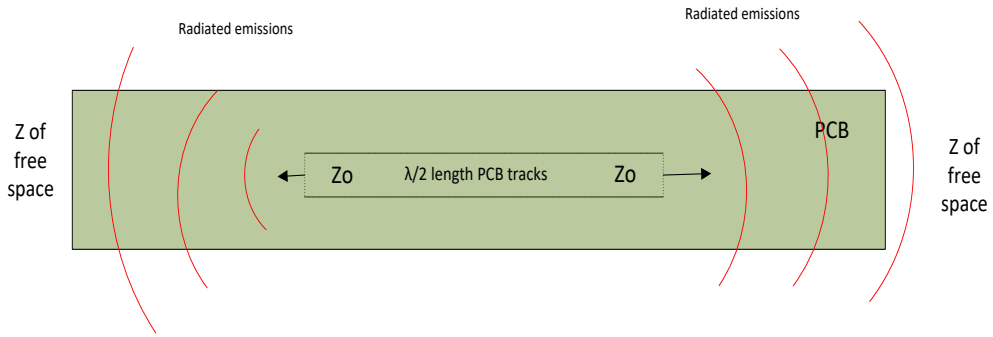




At high frequencies the capacitor can be thought of as a short circuit, which will tend to bring the ground seen by the digital circuit to the same level as the ground seen by the system's main ground. Note a short circuit should not be substituted for the capacitor because it would allow undesirable low frequency ground loop

currents to flow, resulting in magnetic induction (magnetic induction tends to take place at lower frequencies and electric induction at higher ones)

Example 3 – Dipole Antenna established as tracks or planes on a PCB

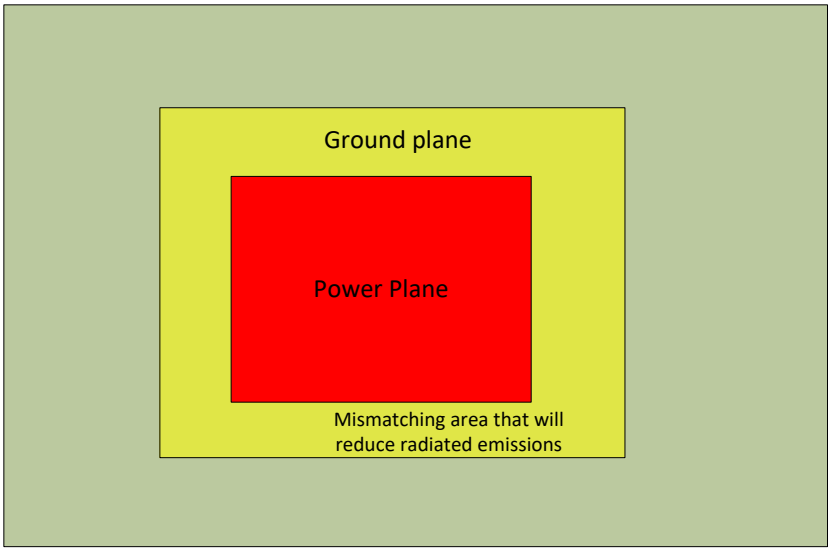


The diagram above stands as an example of both a plan and side view of the PCB; the issue can exist on a single layer or between layers.

Parallel tracks on a PCB can form a dipole antenna as shown in the diagram above: in fact this is the basis of patch antennas that are often purposefully designed onto PCBs. Some suggestions to limit the emissions (not exhaustive) follow:

- Minimise the distance between the tracks, thus reducing the value of Zo. This will cause a greater mismatch between the aerial and the atmosphere (Zo and 377Ω) and reduce radiated emissions.
- Increase the length of the ground track or plane, which will reduce the efficacy of coupling between the aerial and the atmosphere. The diagram below illustrates this for a plane.

Plan view



Concluding remarks on EMC

It is difficult to give prescriptive instructions on this topic, but anyone designing with EMC in mind should realise that it is a balance between **cost, compliance and function**.

Further Investigation

Tim Williams. *EMC for Product Designers,* Newnes

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Definitions

BLE: Bluetooth Low Energy

EMC: electromagnetic compatibility

ESD: electrostatic discharge

FMEA: failure mode and effect analysis

JJ: JonJu Tech Ltd

PCB: printed circuit board without components assembled on it

PCBA: printed circuit board with components assembled on it

Production Release (PR): date at which production is launched without any involvement or supervision from a design authority.

SLEEP: a low current condition that a device can be put into to reduce its requirement for current, and hence longevity if powered by a battery.

WP: white paper