This manual covers the process by which a PCBA is realised from a designer's perspective. It includes advice on EMC and manufacturing to optimise DfM and DfT (design for manufacturing and test)

PCBA Manual

A guide to development

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1. OBJECTIVE

This manual provides a road map for the processes necessary to bring a design into being in the form of a PCBA. Note that this document is expected to evolve – the material for it is extensive.

2. EMC (ELECTROMAGNETIC COMPATIBILITY)

When an electronic device is designed, it may fail to function in the presence of electromagnetic noise from other systems or cause other electronic devices to malfunction because of its radiated or conducted emissions (**EMC failure**).

Electromagnetic noise is classified as being either **conducted** or **radiated**, the former being noise that is conducted along elements of the design, cables, PCB tracks, etc., and the latter noise associated with electromagnetic waves propagated through the atmosphere. Note that conducted noise and radiated noise are bi-directional, i.e. noise created by the equipment under test [EUT] **(emissions)** can contaminate systems outside it with either type of noise, and it can also receive and be disrupted **(immunity)** by noise of these types.

The laws by which electromagnetic waves couple with objects in space are extremely complicated: especially when the systems being modelled are not the regular shaped approximations found in text books (Maxwell's equations mathematically define and solve such problems), but solving real EMC issues depends far more on having the right rules of thumb, approximations, experience and simple circuit models available in one's head. If complex calculations are considered necessary, there are software packages available (https://www.ansys.com/).

It is possible to go to inordinate lengths to limit the adverse effects associated with EMC, but, as is the case with all engineering, performance must be traded against the cost and time necessary to implement the said precautions. Only experience and diligence can be used to do this, but the issue is briefly raised here to make the reader aware of it.

The information in sections 2.1 to 2.11 is sufficient to allow the reader to understand almost any practical EMC problem and its resolution. Section 2.12, *Examples of EMC issues and suggested solutions for the same*, is very far from exhaustive: more examples can be found in Tim Williams (see references), and it is also recommended that the reader adds his own examples to 2.12 as experience allows.

2.1 INTERFERENCE COUPLING MECHANISMS

Whatever the application, an analysis will involve a system of **sources**, **victims,** and **coupling** between the two. The coupling can be via a **direct conductive connection**, such as a cable, by **magnetic induction**, **electric induction**, or by a combination of any or all of the foregoing.

It can be useful to create a block diagram of a system and to identify on it sources, victims and coupling mechanisms. This allows for a systematic approach to problem solving, but it is also worth noting that such diagrams can evolve, e.g. a PCBA will be a system in itself; creating ground maps can also be a useful exercise.

2.2 CONDUCTIVE CONNECTION

As the title suggests, this type of coupling is a physical connection between source and victim, and this link might be a PCB track, component or cable. The first thing that must be emphasized is that

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when dealing with EMC everything has impedance. A copper track on a PCB and a cabled connection have resistance and inductance.

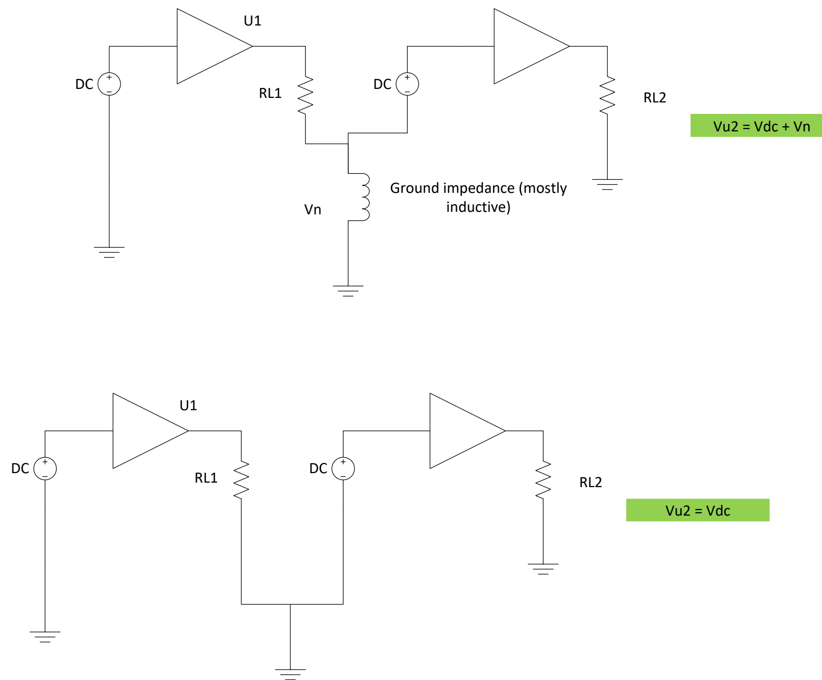

Fig 1

KEY POINTS:

- *Ensure that the physical value of impedance is minimised in cases where connections would ideally have Z=0, e.g. the ground impedance in the first circuit above - use a plane instead of tracks for ground.*
- *Make sure that common return paths for currents are avoided to a maximum degree. The issue is that a noise voltage can develop at a victim simply because two elements share the same ground impedance. This is illustrated in the circuits of Fig 1 and could be caused by a common ground track for both amplifiers in the first circuit, as opposed to both amplifiers connecting to the same ground point at the entry to the PCBA in question, as is the case for the second circuit.*

2.3 MAGNETIC INDUCTION (COUPLING BETWEEN INDUCTIVE LOOPS)

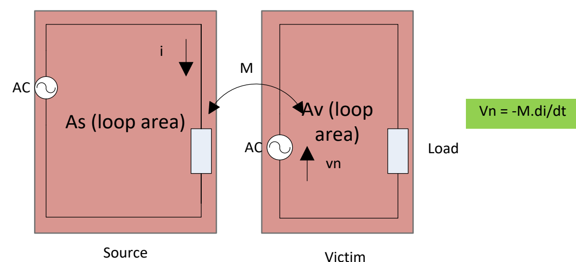

Fig 2

(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)

The area of the loop defined by the source (As), the rate of change of current (di/dt), and the area defined by the loop of the victim (Av), couple to induce a noise voltage (vn) in the circuit of the victim.

A way to reduce the effect described in the previous paragraph would be to introduce of a ground plane instead of using tracks to implement ground, because the loop area is then limited to the thickness between the ground plane layer and the track in question (thickness of just one layer of the PCB, ideally), rather than having the large circuitous route that might be the case with a tracked ground.

The magnetic induction noise voltage in equation 2.3.1 gives all the pointers necessary for the minimisation of magnetically induced noise. Note that this noise voltage (Vn) is independent of source or load impedances in the victim.

$$Vn = -M.di/dt \qquad 2.3.1$$

KEY POINTS:

- ***To minimise M, the mutual inductance, reduce the loop areas of both the source (As) and victim (Av)-see figure 2.***
- ***Increase the separation between the source and victim's loops to further reduce M***
- ***Consider reducing the switching frequency in the source***
- ***Consider band limiting the switching waveform to reduce the maximum di/dt***

2.4 ELECTRIC INDUCTION (COUPLING BETWEEN VOLTAGE NODES)

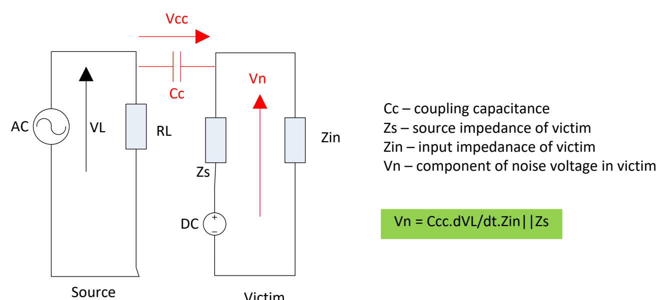

Fig 3

Electric induction involves a capacitive coupling (Cc) between two voltage nodes on the victim and source. This mechanism acts as a current source in the victim (current squirter).

The noise voltage (Vn) present in the victim is derived as follows:

$$Vn = icc.Zvictim \qquad 2.4.1$$

The impedance seen by the noise current (icc) is the parallel combination of source and load in the victim (by Thevenin); and the voltage switched across Cc is VL under the assumption that Xcc >> Zin||Zs (proportion of VL dropped across Cc is much greater than Vn, and therefore approximates to VL).

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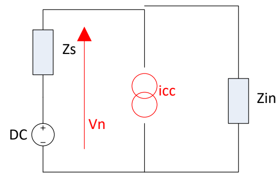


Equivalent circuit for victim with capacitively coupled noise injected as a current

Fig 4

Using the equivalent circuit of the victim, Fig 4, and noting that the current in a capacitor is its value times the rate of change of voltage across it, the noise voltage (Vn) will become by substitution into 2.4.1:

$$V_n = C_c . dV_L/dt . Z_{in} || Z_s \qquad 2.4.2$$

Using this formula it is possible to make some key observations.

KEY POINTS

- ***Reduce Cc by: shielding between source and victim; increasing the separation between source and victim; reducing the surface area of the conducting nodes that form Cc (metallic surface area)***
- ***Reduce the dVL/dt in the source, or band limit it to reduce harmonics***
- ***Assuming Zin>>Zs, which is likely to be the case, reduce Zs (note impedances are in parallel)***

2.5 GENERAL COMMENTS ON COUPLING

A useful deduction, evident from equations 2.3.1 and 2.4.2, is that magnetic induction is independent of the impedances (Zs, Zin) in the victim, but electric induction is dependent on both of them.

KEY POINTS

- ***Vary the input impedance, Zin or Zs, of the victim's circuit to determine if noise is from magnetic or electric induction (if magnetic the noise will not change, if electric, it will.)***
- ***All of the above techniques for modelling EMC issues are conditional on the system in question being of low frequency (length of circuit < $\lambda/4$). High frequency models are covered later in this document.***
- ***Cables couple with electromagnetic noise most effectively when the frequency in question is at the same frequency as the frequency of resonance of the cable (approx. 30MHz).***

2.6 NEAR END AND FAR END CROSSTALK (NEXT, FEXT)

Deriving formulas for near and far end crosstalk using the theory developed in the previous sections is fairly straightforward (see section 10.2.1.1 – Tim Williams), but perhaps not entirely necessary since the principles for reducing crosstalk are simply the reduction of magnetic and electric induction, as described above. There are some observations that may help to identify the source of noise (see Key Points).

KEY POINTS

- ***Note that the analysis in this section is on the basis that circuit length is less than λ/4. If it is greater the high frequency section below applies.***
- ***If FEXT and NEXT are approximately the same but inverted in relation to each other, then it is likely that coupling is predominantly magnetic. If they are the same and in phase it is likely the dominant coupling mechanism is electric induction.***
- ***All the rules for reducing magnetic and electric induction apply to crosstalk too.***

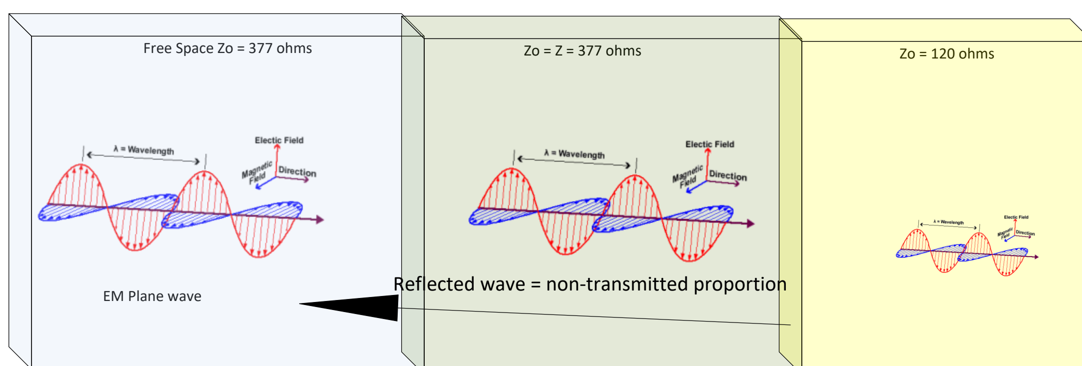
2.7 HIGH FREQUENCY MODEL

At high frequencies (length of circuit >λ/4) magnetic and capacitive coupling cannot be modelled with single 'lumped' components, because under high frequency conditions there are an infinite number of capacitive and magnetic coupling components that are interdependent. In order to cope with this it is necessary to leave the restrictive approximations of circuit theory and enter the domain of field theory (Maxwell's equations), but it is still not necessary to study the complex mathematics underpinning field theory because a few explanations and rules of thumb will allow high frequency systems to be designed and adequately (usually) modelled – certainly as far as most PCBA designs are concerned.

Getting to grips with designing PCBAs with good electromagnetic compatibility requires an understanding of the following concepts:

2.8 CHARACTERISTIC IMPEDANCE AND IMPEDANCE MATCHING

This document assumes the reader has knowledge of transmission lines and basic field theory. Characteristic impedance (Zo) is a property that all high frequency transmission media have, and, if matched and physically connected, i.e. two different media have the same characteristic impedance, then an electromagnetic wave in the first will entirely pass into the second without reflection. Furthermore, if the transmission media have different Zo then only a proportion of the wave will be transmitted and the balance reflected, the limiting cases being total reflection for a line terminated in an impedance of Zo = ∞ or Zo = 0. These properties are essentially frequency independent, providing the circuit length > λ/4. The principles above apply to propagation over free space and propagation over man made media such as coaxial cables, PCB striplines, etc. The diagram below illustrates this.



The characteristic impedance of man-made transmission lines, such as PCB stripline or coaxial cables, and assuming lossless lines, are determined by the geometry and dimensions of conductors,

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insulators and the properties of the materials – principally the insulation permittivity. Calculation and/or measurement of such values are beyond the scope of this report.

2.9 NEAR AND FAR FIELDS

The EM waves in the section above are known as plane waves (E field [red] is perpendicular to the H field [blue]). These exist in free space and correspond with Zo = 377 ohms, which is all fine as long as the analysis is taking place in what's known as the **far field.** The far field is the propagation space at an appreciable distance from the source of the EM wave, at which distance, all other things being equal, electromagnetic waves will be plane. The **near field** has different properties that are not easy to predict and result in wave impedances that can be anywhere between about 30 and 3000 ohms, which means unexpected reflection and transmission may result.

It really is very difficult, and likely pointless, to try and predict exactly what is going on in the near field. Most near field effects are caused by **common mode** noise, which is covered in the following section: it is simply necessary to take all possible steps to reduce common mode noise.

KEY POINTS:

1. ***According to Maxwell's equations the transition from near field to far field occurs at λ/2Π. This gives the designer a guide upon which to estimate whether whatever conclusions he is coming to apply to the near or far field.***
2. ***Note that cables magnetically couple at lower frequencies (<30MHz) and are most receptive to coupling at frequencies at which the cable resonates.***

2.10 COUPLING MODES (DIFFERENTIAL, COMMON AND ANTENNA MODES)

It is very important that engineers thoroughly grasp the notions of common, differential and antenna mode noise coupling – common mode noise is particularly important when considered with respect to EMC. This section is all about magnetically induced currents – suggest re-read of section 2.3 before assimilating that which is immediately below.

2.10.1 DIFFERENTIAL MODE NOISE

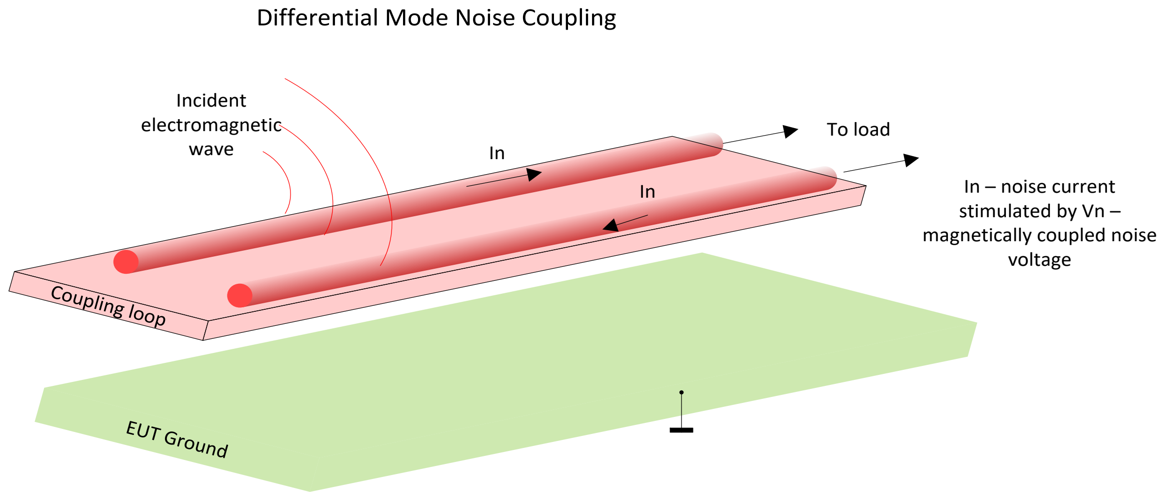

Fig 5

Differential mode noise is the current induced by an electromagnetic wave that couples with the signal/power circuitry (cable in Fig 5) **only.** This creates a noise current in the loop according to the principle explained in section 2.1.3 (magnetic coupling), and this current will flow around the loop, thus making it have a 'go' and 'return' path, but this path is not necessarily in sympathy with the direction of any signal current flowing in these cables.

2.10.2 COMMON MODE NOISE

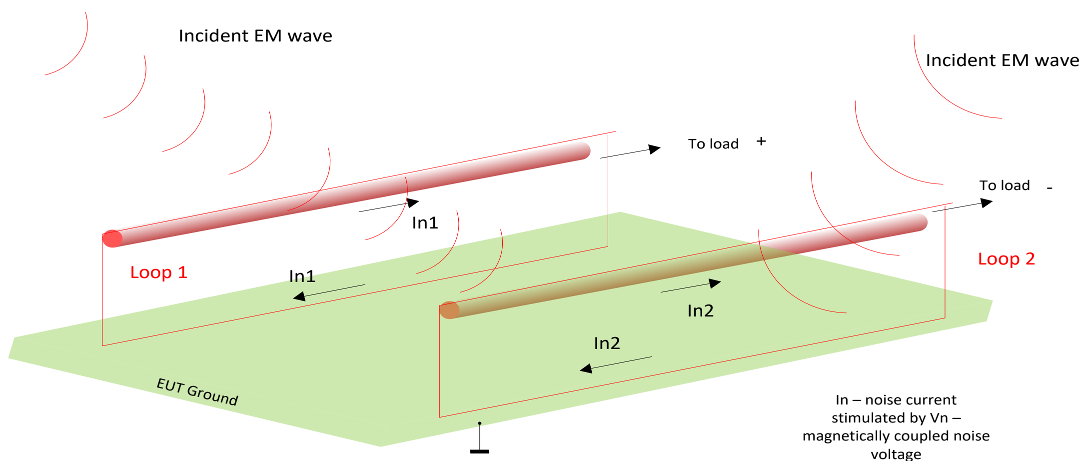

Fig 6

Common mode noise is generated when an external magnetic field couples with the loop set up by ground and each signal/power carrier (cable in Fig 6) independently, which results in currents in the cables that flow in opposition to each other: but these should not be thought of as currents that are on a collision course with each other in the load - the coupling is relative to ground rather than through the load. It is a mistake to think of common mode currents flowing in opposition through the load, they aren't. They are flowing in a loop relative to ground. Also note that two EM waves have been drawn, but it may be the same EM wave that couples with both loops.

2.10.3 ANTENNA MODE NOISE

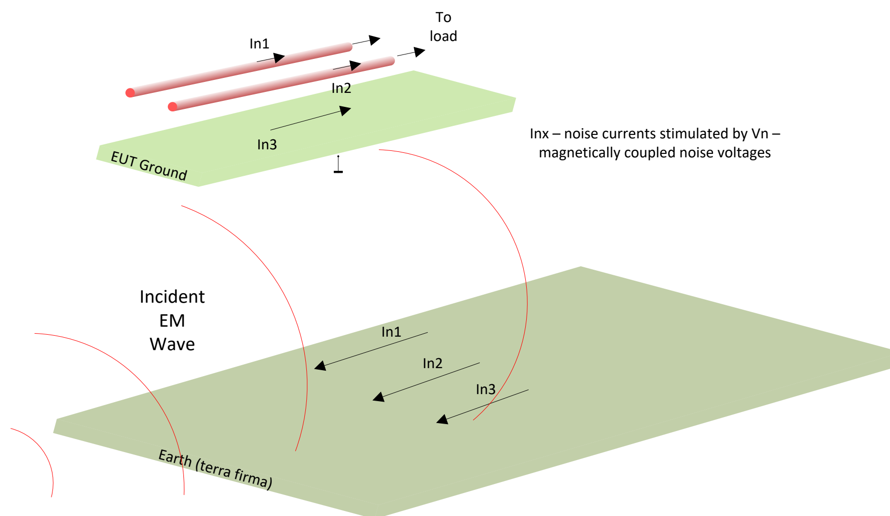

Fig 7

Antenna mode is similar to common mode in that currents flow relative to ground reference, but that reference is the ultimate ground reference –terra firma. The incident EM wave couples with loops set up by the EUT and terra firma, in this case 3 loops inducing currents In1, In2, In3. The principle is the same as the common mode case except the low side reference is terra firma (Earth) instead of the EUT ground.

KEY POINTS:

- ***Common mode noise is the dominant issue in most cases when considering EMC***
- ***Don't become confused by signal currents, they are essentially independent of these mechanisms, although there is a mechanism by which common mode noise can be converted into differential mode noise (see section 2.12)***

2.11 MAINS ELECTRICITY

The main things to consider when assessing mains supply to a product that is to be EMC assessed are: the quality of the mains supply in the first place which, although variable, is outside the control of the electronics engineer; the propensity for the mains to become contaminated with common mode noise from the EUT (conducted emissions); and the ability of the EMC filtering and

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power supply design to reject noise such that it doesn't appear at the input of the EUT (equipment under test).

It is recommended that fully approved, commercial PSUs (the choice may be a function of the EN standards that are to be tested against) are used with differential and common mode filtering on the mains input to the EUT.

If the reader wishes to delve into issues with the mains supply Tim Williams (in references) covers them admirably.

KEY POINTS:

- ***Use commercial EMC/EMI mains noise suppression products, or discrete component filters, if such are needed for the product. These assist with passing conducted emissions and immunity tests.***
- ***Use fully approved power supplies from reputable suppliers, and the model of supply chosen may be determined by the EMC standard it is necessary to pass.***
- ***Note that whilst the PSU supplier has a responsibility to provide a product that will reject noise it sees at its input, it doesn't have a responsibility to reject noise that an EUT might push back onto the supply (impossible to do this because the PSU designer can't know the details of loads that might be applied). The CMRR (common mode rejection ratio) should not be considered as reciprocal. The upshot of this is that the PSU should not be considered as a panacea for rejecting conducted noise emanating from the EUT - the product designer must take responsibility for it.***
- ***Use transzorbs and other protection and clamping systems to protect the design from unexpectedly high voltages (surge tests that simulate lightning strikes on cables are done as part of standard EMC testing), over and above the filtering offered by the commercial EMC filter.***
- ***Design firmware such that it will always reset and recover after noise that could cause a microprocessor failure has ceased(watchdog timers (external better - but use both software and hardware WDTs if appropriate), write hardened firmware, etc.).***
- ***Consider the use of ferrites both in the design of the product and in the external cabling to suppress noise, if necessary (note external ferrites are often the means by which a product is nudged into a condition that permits a pass).***
- ***Note that inductors have most effect at lower frequencies and ferrites higher ones.***

2.12 EXAMPLES OF EMC ISSUES AND SUGGESTED SOLUTIONS FOR THE SAME

There are a multitude of noise scenarios and it isn't practical to list them all and explain how using the theory above can overcome them, but it is possible to use the methods to work out solutions for a very wide range of issues. There are a few examples below which should help to illustrate this.

There is no substitute for experience so the advice of this report is to grasp every opportunity possible to work on products needing EMC approval. With the foregoing theory it will usually be possible to work out the cause of noise and find ways to minimise it.

Example 1 – Common Mode Noise causing Differential Mode Noise

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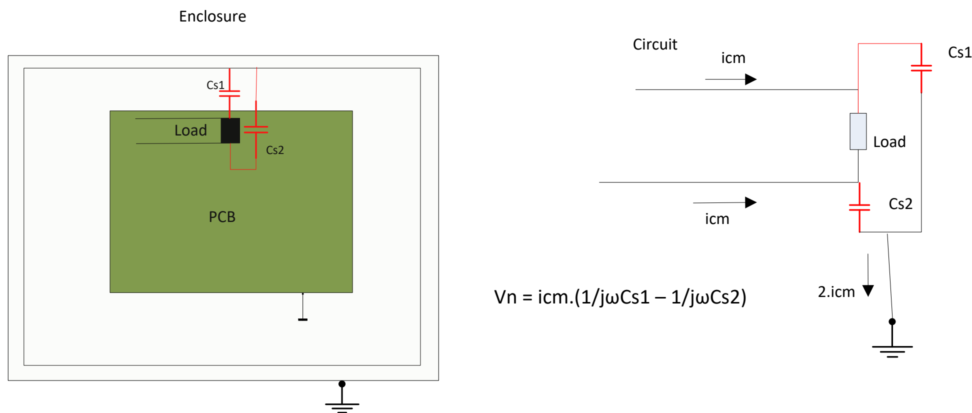
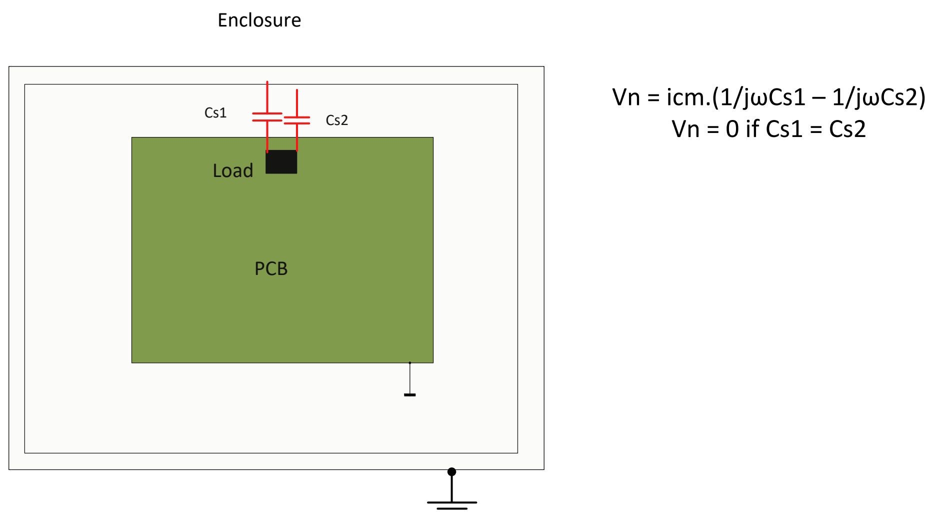
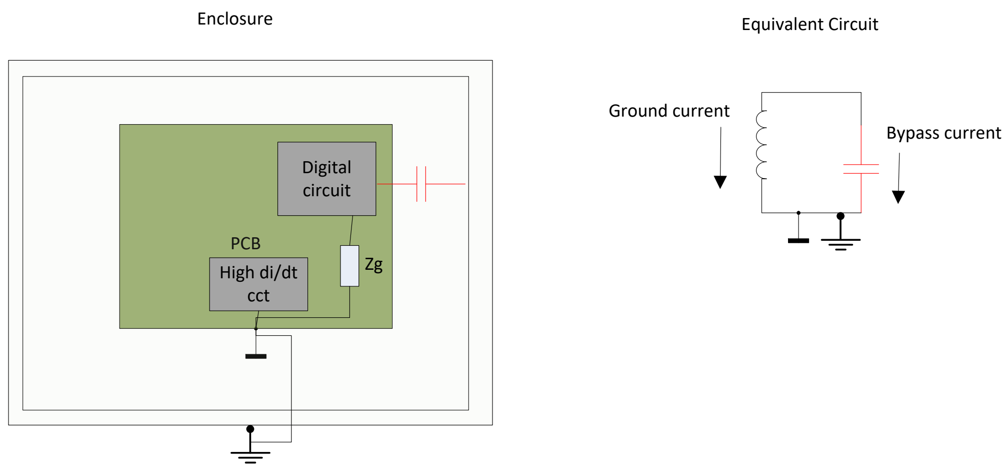


Stray capacitance between each end of a load and the case can cause common mode currents (icm) to generate differential mode noise (vn) across a load as above: because Cs1 ≠ Cs2. This can be improved by physically turning the load through 90 degrees as in the diagram below (result is Cs1 = Cs2).



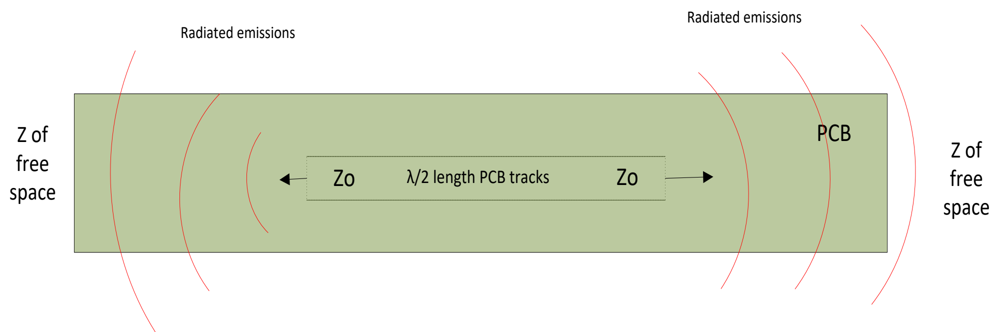
Example 2 – Using Casing Capacitors to Circumvent high Ground Impedance on a PCB

Ground paths, tracks and planes on a PCB have inductance. At high frequencies the resulting impedance can be such as to introduce unacceptable differences in the ground potentials at various points around a PCB. Ground inductance is usually of the order of tens of nanohenries, so noise in a 20nH ground carrying 100μA might result in a noise voltage of 62μV at a frequency of 5MHz (Vn = ωL.i). It becomes necessary to find ways of reducing the effective ground impedance when noise voltages generated in this fashion are unacceptable, and this is often done as shown in the diagram below.



At high frequencies the capacitor can be thought of as a short circuit, which will tend to bring the ground seen by the digital circuit to the same level as the ground seen by the system's main ground. Note a short circuit should not be substituted for the capacitor because it would allow undesirable low frequency ground loop currents to flow, resulting in magnetic induction (magnetic induction tends to take place at lower frequencies and electric induction at higher ones)

Example 3 – Dipole Antenna established as tracks or planes on a PCB



The diagram above stands as an example of both a plan and side view of the PCB; the issue can exist on a single layer or between layers.

Parallel tracks on a PCB can form a dipole antenna as shown in the diagram above: in fact this is the basis of patch antennas that are often purposefully designed onto PCBs. Some suggestions to limit the emissions (not exhaustive) follow:

- Minimise the distance between the tracks, thus reducing the value of Zo. This will cause a greater mismatch between the aerial and the atmosphere (Zo and 377Ω) and reduce radiated emissions.
- Increase the length of the ground track or plane, which will reduce the efficacy of coupling between the aerial and the atmosphere. The diagram below illustrates this for a plane.

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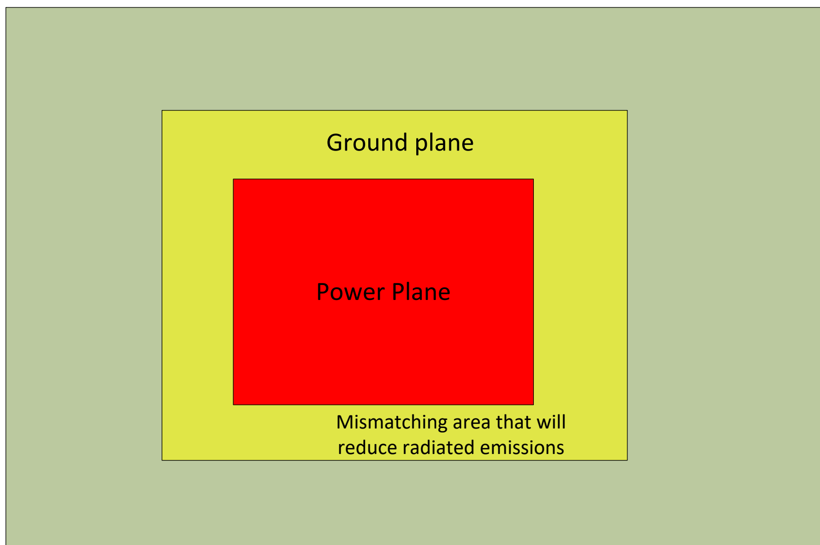
Plan view



2.13 CONCLUDING REMARKS ON EMC

It is difficult to give prescriptive instructions on this topic, but anyone designing with EMC in mind should realise that it is a balance between **cost, compliance and function**.

3. ESD (ELECTROSTATIC DISCHARGE)

The problems that ESD can cause for electronic circuits are probably some of the most misunderstood and misinterpreted in the electronics engineering profession. The issue is a fine example of the adage ‘a little knowledge is dangerous’. The following is not an exhaustive description of the topic, but it should give a sound basis upon which the interested reader can study further without fear what they’ve learned is mythical: and most importantly it provides the material necessary to recognise the myths surrounding this topic.

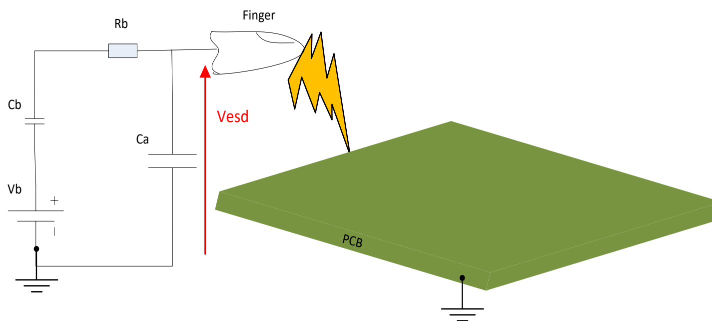


Fig 3.1

There are two vessels for the charge that result in a damaging discharge: the human and the atmosphere. The latter is very important, but usually overlooked.

Human beings build up charge through friction and with their clothes, i.e. via the triboelectric effect. This is mitigated in industrial environments by: making people in the environment wear clothes that are least likely to generate charge; using wrist straps and footwear that dissipate charge when a suitable discharge path exists; providing the discharge path using dissipative mats,

floors, furniture, etc.; and ensuring that sensitive components are transported and stored in dissipative bags and containers. The circuit in Fig 3.1 illustrates the charged human via Vb, Cb and Rb, which is a system with a relatively long time constant and lower peak voltage when compared to its atmospheric counterpart (Ca with a very low indeterminate value of Ra [resistance limiting discharge by the atmosphere]).

The atmosphere becomes charged and it is through this that the most damaging ESD occurs, and it is this that is commonly misunderstood. The circuit of Fig 3.1 illustrates this via Ca and Vesd. Ca is the capacitance of the air between the conductor formed by blood flowing in the victim's finger, and the insulating properties of the skin and air between this conductor and the conductor on the PCB that suffers the electrostatic discharge. The charge is equal to the Vesd x Ca. The resulting discharge has a high peak voltage and short time constant. Since the discharge is principally a function of the charge held in the atmosphere, no amount of ESD clothing, equipment or training for people will prevent it (the most effective way to reduce it is to introduce de-ionising machines in the work place [note air conditioning units charge the atmosphere quite effectively]). Charge tends to accumulate in the atmosphere when humidity is low (dry air), and by monitoring humidity it is possible to identify times at which the risk of damaging atmospheric discharge is present: handling of PCBAs should cease when this is the case. When humidity is high the atmosphere is less likely to hold significant charge, but the likelihood that discharge will occur is higher (wet air). This suggests that there should be both lower and higher trigger values of atmospheric humidity outside of which no handling of PCBAs should occur.

Electronic chips were relatively susceptible to ESD decades ago but modern chips usually quote a 'body model voltage' which is normally in the region of 2kV. Good designs also include protective measures outside the chips such as clamping diodes and transzorbs so that failure is now much rarer than it used to be, but it still occurs and it would be remiss of a designer or manufacturer to not be seen to be taking to steps to reduce the effects of ESD.

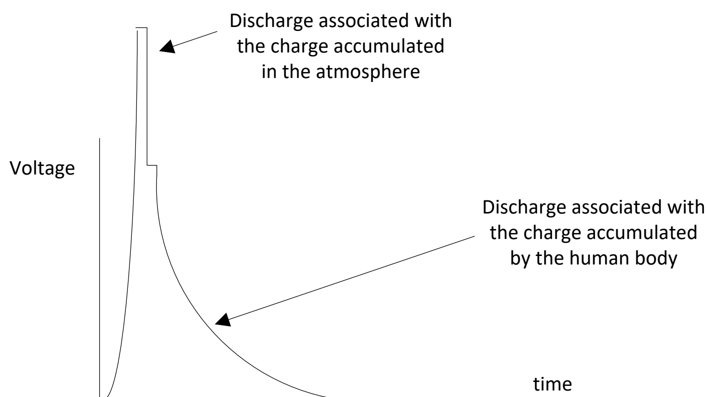


Fig 3.2

KEY POINTS:

- ***Damage from ESD is insidious. It may destroy a component instantly and hence make known the fact that a PCBA is compromised, but it can also simply shorten the life of a component.***

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- ***The worst damage from ESD occurs via atmospheric not human charge, and this is usually controlled by setting humidity limits outside of which no work should be carried out on PCBAs, and the introduction of de-ionising equipment should be added to a minimum level of human protection.***
- ***All reasonable steps should be taken to reduce the risk of discharges from humans (ESD reducing clothing and equipment, etc.)***
- ***There are international standards for the control of damage from ESD – follow these (BS EN 61340-5-1:2016).***
- ***Note that the addition of conformal coating can significantly improve the level of resistance to ESD. For the discharge to occur the conformal coat would need to physically break down, and this is unlikely because conformal coats are designed to have high dielectric strength.***

4. PCBA MANUFACTURE

Before launching into the details of PCB and PCBA manufacture, it is necessary to state the reasons for emphasizing these details to design engineers.

Whilst manufacturers are often capable of coping with all sorts of variations and combinations in designs, it is a mark of an inexperienced designer engineer to test such manufacturers limits needlessly. If a design requires greater care in order to reach tighter tolerances, or is made to suffer such things as poor copper balance (see glossary), then the resulting product will likely be more expensive and prone to lower yield.

The following section runs through the main processes necessary for the manufacture of a PCBA. It is designed to give the reader the following:

- A perception of the process
- An appreciation of the limiting factors of production
- Guidelines on DfM (design for manufacture)
- A brief overview of testing

The coverage should not, however, be taken as a thorough production engineering treatment, or to cover the processes in the exact order that they might happen. It should further be noted that the detail in the following sections is deliberately light, only being what a design engineer, rather than a production engineer, might need. The following only covers rigid PCB and PCBA production.

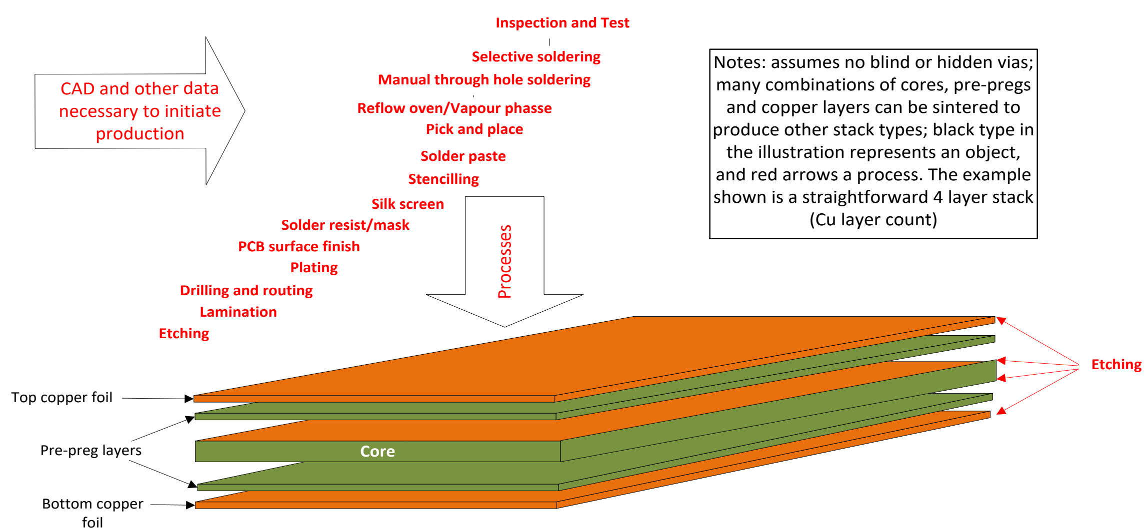
The diagram below shows all the processes (in red) and these are explained in more detail in the sections that follow.

The PCBA layer stack diagram below identifies the physical elements (in black print in the diagram), and the sections below describe each process (in red print in the diagram) in detail. The paragraph in italics below gives a necessary overview of the processes (note there are permutations and combinations of the processes that mean it isn't possible to state them in a fixed order [the order implied by the following paragraph is not necessarily practical]).

The basic PCB is made up of laminates that are called cores, pre-preg layers and foils. The foils are usually made of copper and the cores and pre-preg of glass reinforced plastic (normally named FR4), but the core will also have foils pre-attached to its bottom and top. Each copper layer or foil must have the copper that's not needed removed such that only the tracks, pads and planes that are needed for the PCB are left. This is done by attaching a carefully constructed resist layer over

(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)

the foil such that the proposed tracks and layout will be protected from the electrolyte when the etching process takes place. The etching process will take place multiple times as the laminate builds up. After each etching stage the laminates are all formed togehter by using sintering (temperature and pressure). The pre-preg layers are semi-cured FR4 that act as a bonding material when subjected to the sintering temperature and pressure, whereas the core is already fully cured. When the entire stack has been made the panel, which will probably contain many PCBs, has all the necessary holes drilled and slots routed (milling process). The holes must then be plated to for the PTHs (plated through hole), and the plating process will supplement the thickness of un-etched Cu on the top and bottom layers. In addition to this pads are tinned to make the soldering process work properly, following which, and there are different surface finish processes, the areas intended for soldering are coated in a very thin layer of silver (silver immersion) which is added to stop oxidisation of the tin coated copper before soldering has been completed. The solder resist or mask stops solder from sticking to areas where it is applied, and it is this solder resist that gives a PCB its colour. Following this the silkscreen is applied (the white printing which identifies the component designators and is used for all other printing on the PCB). Finally, the panel is routed (milled) such that each individual PCB can be pressed out of the panel, i.e. the PCBs are cut out almost completely but for small notched areas, which are called rat bites. At this stage the PCB is complete and the assembly process starts. It is first necessary to cut a stainless stencil that has holes in it that align exactly with every spot on the PCB that will require solder, then solder paste, which is just a machine friendly form of solder, is forced through the holes onto the PCB, and the stencil removed. Pick and place machines then place all the components on the PCB, following which the PCBs pass into what's called a reflow oven, which melts the solder and virtually completes the process. There may be some through-hole components that require soldering after the SMD (surface mount device) work has been done. The PCBA is then ready for test and shipping.



4.1 THE INPUTS NECESSARY FOR MANUFACTURE

The data that's necessary to manufacture a PCBA is generated by CAD software, eg. Altium, PADS, Easy PC, etc. This section doesn't cover the design of electronics so the details of that process

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aren't considered. In order to purchase a PCBA from a manufacturer it is necessary to provide the following data:

- **A BoM (bill of materials)**. This is a list of all the components that are to be attached (usually soldered) to the PCB; their designators (how the components are identified on the board with the silk screen – R1, C1, D1, U3, etc.); part numbers, both for the supplier and the manufacturer; identification of both supplier and manufacturer; quantities of each unique component; and comments such as DNF – do not fit – if it is relevant. This data is usually presented in a spreadsheet, but the CAD software can usually auto-generate it.
- **PCBA Manufacturing Files.** It is necessary to send details of what copper to etch and what not to, i.e. the copper tracking and plane definition for each copper layer; where to drill holes for vias, etc.; and x,y data so that the pick and place machine can place the components in order to make the footprints match up with the pin configurations of the components. This is data is usually auto-generated by the CAD software and will be in the form of either an ODB++ folder or Gerber, NC drilling and X-Y data files. Unless the designer has special requirements it is best just to allow the default settings to apply, and generating the above files then becomes simply one or two button pushes on the computer.
- **PCB board specification.** The mechanical details that are not usually defined by the Manufacturing files must be stated separately, usually in a PCB specification text file. The following illustrates the minimum extra detail that is required:
    - **The Cu weight** (this is in ounces/ft^2). 1oz Cu is the normal, but up to 4oz Cu may be specified in cases in which a PCB may be required to carry significant current.
    - **The surface finish.** Bare PCBs with simply open copper or tin on their pads will oxidise quite quickly, and this is a problem because the oxidised copper pads will not solder properly. For this reason it is normal to put a protective layer over the pads that are to have a soldering process carried out on them. Either a very thin silver or gold layer is applied, and this known as **silver immersion** or **gold immersion** respectively. There is an alternative process called HASL (hot air solder level), which is a process by which the PCB is immersed in a lead/tin alloy and excess alloy is removed by high pressure air. There are other treatments, but the above are the most common. It is simply necessary to state that either Au or Ag immersion is required.
    - **Conformal coating.** PCBAs are sometimes coated in a high dielectric strength, water proof layer. This is known as conformal coating. This layer should only be applied if it is required for some engineering reason – moisture protection, added barrier against ESD, etc. It will be necessary to generate a document specifying which, if any, components are to be masked so that they are not covered in the coating material, eg. a connector. It also should be noted that PCBAs that have had a conformal coating are almost impossible to re-work and re-solder should modifications be necessary – don't conformally coat a prototype PCBA.
- **Firmware specification**. Many PCBAs have chips on them that need to be programmed. Unless it is the customer's intention to program the PCBAs himself, it is necessary to provide object code (hex file) and possibly programming instructions.
- **Special manufacturing instructions**. If there are any extra requirements, for example a small amount of mechanical assembly, instructions must be written.

All the other detail should be available via the information in the manufacturing files and BoM.

The final thing to note is that all CAD software has DRCs (design rule checks) and these allow the user to set limits such that manufacturing limits are not exceeded, e.g. minimum track gap

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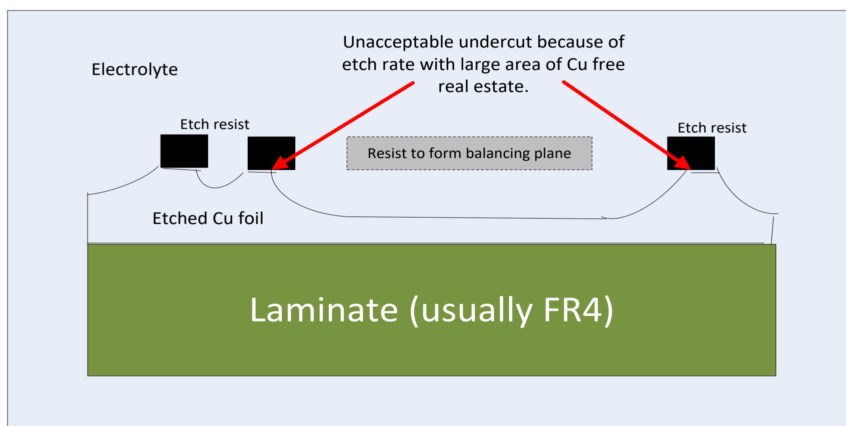
and width. It is necessary to make sure that the CAD has been configured such that it reflects the manufacturing performance of the manufacturer. The following sections should help to ensure this is the case.

KEY POINTS:

- ***To order a PCBA the minimum it is necessary to provide the manufacturer with: a BoM (bill of materials); a board (PCB) specification; CAD manufacturing files; and the number required.***

4.2 ETCHING

Electrolysis is used to etch copper from foils that is not wanted, and this process is known as chemical etching. This is illustrated in the diagram below, which shows a PCB immersed in an assembly that forms an electrolytic cell that causes depletion of copper.



As the diagram above shows, the etching doesn't take place evenly. Areas that are free of resist etch more quickly than those having a greater nearness of resist. There are two reasons for this: diffusion and electrolyte flow, but the effect of flow alone is sufficient to explain why this occurs and how it can be improved. It is necessary to improve the **Copper Balance**, which, as the name suggests, is the design norm by which expanses of a PCB are designed so that there is an even spread of Cu on the PCB. If this is not the case, as above, then differing etch rates occur. The reason flow causes this effect can be understood by drawing an analogy with a river. Water flows fastest in the centre of a river because the resistance to flow is set up by friction with the banks and bottom. The same effect occurs with etching because the resist slows the flow of electrolyte and consequently impedes etching, but the open areas have a faster flow of electrolyte and hence etch more quickly. The problem with this is that over etching can occur as marked by the red arrows in the diagram above. This can be mitigated by putting a redundant copper pour in as shown in grey.

KEY POINTS:

- ***Don't design PCBs with large areas with no copper in them for the reason explained above. Ensure designs have a good 'copper balance'. Copper Balance means making the spread of copper even throughout a layer; there should be no 'copper deserts'.***

4.3 LAMINATION

(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)

As stated in the introduction to PCB manufacture, PCBs are made by sintering layers together. The pre-preg layers then cool and cure to hold the PCB together. Obviously, the reverse of this process can occur if the PCBs are used in at a temperature such that the pre-preg layers soften and delamination occurs. The temperature at which this happens is known as the glass temperature (Tg – glass temperature), which is a property of FR4 which is widely published.

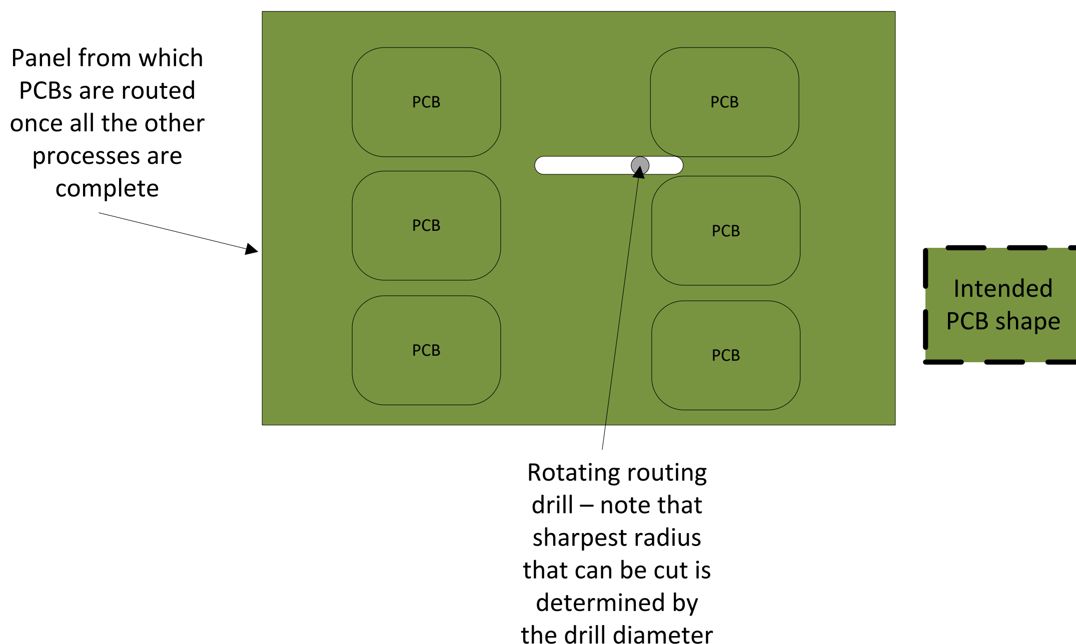
As can be imagined, the tight tolerances and miniature components mean that lamination, etching and drilling must be very precisely aligned. The design engineer must aid this process by putting fiducials in his design, which are basically dimensioned pads with no tenting upon which the manufacturer can register and align the components. The generation of fiducials is widely covered elsewhere - search Google.

KEY POINTS:

- ***Make sure the PCB is being used at temperatures well below the glass temperature of the material used for laminate insulation.***
- ***Ensure fiducials (tiny untented pads that are used to register the position of the PCB/PCBA) are included in the design***

4.4 DRILLING (LASER AND MECHANICAL) AND ROUTING

In order to form PTHs and slots holes must drilled and/or milled in the PCB in very precise positions. These can be done using traditional drilling machines, or with more modern laser cutting devices. Slots and the outline of a PCB from its panel are cut using a process called routing, which is really just a process that mechanical engineers would call milling. Since routing uses a drill, albeit a very small one at times, it must be realised that true right angles can never be produced as part of the shape of a PCB. The diagram below illustrates this.



The principle illustrated in the diagram above would apply to the PCB shape and any slots or other geometric features of the PCB as well.

KEY POINTS:

(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)

- ***Make sure, during the CAD design process, that you aren't suffering from 'CAD eye', i.e. it is easy to draw in CAD but impossible to make.***
- ***If your CAD design package allows it, ensure that the DRC (design rule checker) will stop impossible shapes being routed.***
- ***Whilst laser technology allows for microvias and very accurate and minute forming, it is not suited to routing or being used to remove large quantities of material. This is the reason laser routing is not a process one can expect to easily find - it would take an age and would likely stress the machinery involved.***
- ***Note that laser drilling allows for drilling very accurately to partial thickness depths, e.g. for implementing a blind via.***

4.5 PLATING

Plating is very much in the lap of the manufacturer; let the experts take care of their own core skills. It is nevertheless useful for a designer to appreciate limitations that could affect his design. As long as the manufacturer produces good quality PCBs meeting acknowledged standards, e.g. the IPC standards, and the design isn't one involving very high frequency signals or high currents, then there is almost certainly no reason for a design engineer to worry about the process of plating.

For the high frequency case it is geometric thicknesses and their consistency that are the concern. The characteristic impedance, described in the EMC section, is critically dependent on the properties of the materials used, particularly those concerning insulation, and the dimensions of all the constituents of the PCB transmission line, e.g. stripline. Plating cannot be applied evenly, there will be both thick and thin spots.

Copper Weight is another factor that will have an influence on plating. Obviously, increasing the copper weight will improve a PCB's ability to carry current, and plating is usually the vehicle through which this is achieved. It is not necessary for the design engineer to know a great deal about the process, but he must be cognizant of the term Copper Weight and what it means. Copper Weight is the weight of Cu per square foot. The normal value for most PCBs is 1oz, but 2, 3 and 4 oz may commonly be used for applications that must carry high currents on their PCBs.

KEY POINTS:

- ***Where possible avoid vias on high frequency nets, the geometric anomaly and plating thicknesses will cause reflections***
- ***Where possible avoid placing high frequency signals on tracks that are plated (the top and bottom layers are normally plated) for the reason in the previous bullet point. If said tracks are on a Cu foil much better dimensional stability will be achieved.***
- ***Note that there is a trade-off between Copper Weight and track and gap minimum widths. Heavy plating makes it difficult to maintain very fine gaps between tracks. It may be prudent to make sure different layers carry the different types of load, e.g. signals, power.***

4.6 SURFACE FINISH (INCLUDING CONFORMAL COATING)

The soldering process requires that the surfaces being soldered aren't oxidised, and copper and tin will oxidise over time. To prevent oxidisation a layer of inert material is coated over all surfaces that require to be soldered. The metals that are used for this are tin, palladium, gold and silver. It should be noted that resistance to oxidisation is not the only criterion, e.g. palladium and gold might be used where press fits are required. To use generic terms gold and silver immersion are

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available, but other materials like palladium and tin may be part of the surface finish treatment. There is another method known as HASL (hot air solder level) that involves dipping the sample in hot solder and using a hot air gun to remove excess.

HASL is falling out of fashion but the others are regularly used. The thicknesses involved are just a few µm with gold or silver immersion, but HASL may vary between 2µm and approximately 40µm and isn't even over its surface.

Conformal coating is a process by which a thin layer of high dielectric strength plastic is sprayed over a PCBA, noting that parts that don't require it can be masked. Using it will provide the following advantages:

- It will improve a PCBAs ability to withstand vibration and shock without having components fall off the PCB
- It is an extra protection against ESD, introducing a very high resistance path that will greatly decrease the likelihood of a breakdown discharge from the atmosphere because the coat must also breakdown to cause ESD, and this is unlikely since such coatings have very high dielectric strength.
- It is a good barrier against moisture and dust
- It can protect against electrolytic corrosion because metallic parts cannot connect through an electrolyte, like water, and therefore corrosion that results from the electrochemical series is avoided. To make this clearer, a PCBA might have both copper and aluminium in it, and these two metals are well separated in the electrochemical series, so, in the presence of an electrolyte like water, corrosion will occur. Conformal coating removes this problem because the two metals are not connected through an electrolyte.

KEY POINTS:

- ***If your application is ordinary in nature choose silver immersion and if not, gold.***
- ***Modifying PCBAs after conformal coating is not practical. Don't conformal coat PCBAs that are likely to need modifications, i.e. prototypes.***
- ***Consider conformal coating for protection against chemical, ESD, environmental and physical constraints***

4.7 SOLDER RESIST/MASK

Solder Mask is a material treatment applied to PCBs with the primary purpose of preventing the adhesion of solder during the PCBA assembly process, but it also serves as a plating resist for surface finishing and its physical properties are often required for the PCBA's final application.

The solder masking process is the one that is responsible for the colour of a PCB.

(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)

Photolithography is used to develop solder mask free areas, and this is a process requiring considerable skill, but the designer should probably leave this in the hands of a competent manufacturer.

The issues that a designer should consider are as follows:

- Solder masking is defined in the CAD package used. In other words PTHs, Pads, pins, etc., all have solder mask areas defined for them. Most CAD packages have default settings for this so the designer that has designed an uncomplicated PCBA may not have to worry – but should check anyway.
- Pay particular attention to fine pitch ICs and the need for solder mask dams in between the pins. Again, the CAD package should have these things set up as standard but it bears checking.
- Tenting, which is the covering of vias with solder mask, can be important, particularly if there is an intention to put a via in a pad (which is not recommended for PCB Train).

KEY POINTS:

- ***Unless there is a good reason not to, pick green for the PCB colour. Most PCBs are green and it is likely that quicker delivery and possibly a better price will result if green is chosen.***
- ***Make sure that the CAD package that is being used has configured the mask layer as you expect. Note this may be done feature by feature, e.g. pads, PTHs, etc.***
- ***Ensure that solder dams (lines of solder mask between pins of ICs) are present. Failure to do this can result in unexpected shorts between pins because of solder bridges.***

4.8 SILK SCREEN

Silk screen is the process, usually in white on a green PCB (black on a white PCB), which shows the writing that identifies the component's designators and deals with any and all labelling on the PCB. There isn't much reason for a designer to be overly concerned with this process except in respect of the 'Key Points' listed below:

KEY POINTS:

- ***Make sure you aren't suffering from CAD eye. The print must not be so small on the PCB that it is either illegible or without sufficient definition.***
- ***Position labels for designators such that components and other features when assembled will not obscure or hide the designator. There are intuitive techniques for doing this like making a silk screen line act as a pointer.***
- ***Make sure all polarised components, like electrolytic capacitors and LEDs, have their polarity clearly marked.***
- ***Pin 1 of IC's must be clear because rotated chips will at best not work, and at worst permanent damage to the PCBA may result.***

4.9 STENCILLING

Stencilling is also one of the processes about which a design engineer should be aware but need not be an expert. This is the major process that is the first stage in the assembly of the PCBA from the PCB. Solder needs to be applied to all the pads and connectors that require it, for SMD assembly,

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and the accurate positioning of this solder is achieved by using a stainless steel stencil. The stencil is cut such that there is a hole for each and every SMD area that requires solder (the machines that cut stencils use lasers that are programmed from Gerber data). Cutting stencils that are fit for purpose has all sorts of arcane information associated with it, e.g. 'wendy house' pad shapes that improve the efficacy of the process, different thicknesses of stencil to allow for wide and narrow pitches between pads, stepped stencils for designs that have both wide and narrow pitches on the same layer. The intricacies of stencilling do not, for the most part, need to bother a designer other than for the key points listed below.

KEY POINTS:

- ***As far as the design allows, try to keep fine pitches and small pads and wide pitches and large pads on different layers. This should tie in with the needs for copper balance.***

4.10 SOLDER PASTE

Solder paste is, as the name suggests, simply solder in a form that makes it relatively simple to apply to SMD PCBs. There are different types of paste suited to different tasks, but design engineers don't need to be overly concerned about these. The solder paste is wiped over the top of the stencil in, a windscreen wiper kind of action, and then down onto the appropriate places on the PCB through the stencil. This, again, is a process the design engineer doesn't really need to know a lot about.

4.11 PICK AND PLACE

Pick and place machinery is robotic machinery that automatically picks components from reels and places them in the correct position on the PCB after the solder pasting process. The solder paste, through a combination of surface tension and stickiness, holds the components in place loosely.

The choice of components and the information that's supplied with the BoM is of more importance than the pick and place process itself – leave the process to the experts.

The following subsections cover features that can help to very much improve DfM

4.11.1 STANDARD STOCK

It might be thought that a good design specification (particularly the BoM) would contain prescriptive part numbers and descriptions for every component on the PCBA. This would be a reasonable but erroneous conclusion.

Consider a design in which a capacitor had been specified as a particular manufacturer's part (all numbers identified), but the distributors happen to be out of stock and the lead time for a replacement is six weeks. Further consider that the capacitor in question is a standard 0402 ceramic 0.1μF capacitor being used as a decoupling capacitor, which is entirely mundane and for which there are numerous substitutes. The design engineer that has taken this route will then have to cope with one of the following avoidable issues:

- An unscrupulous manufacturer might simply make a substitution without informing the designer. Whilst this shouldn't cause a problem, it must be considered that most manufacturers aren't design engineers and the substitution might be inappropriate.

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- A poor manufacturer may simply not fit the part and not tell the design engineer, which probably wouldn't stop the product working but would certainly affect the integrity of the design (EMC issues might flush the omission out at a later stage – at relatively high cost).
- An unacceptable delay in production might result whilst the specific part is ordered against an onerous lead time.

All of these scenarios are avoidable because such a standard part fitted to implement such a mundane function need only have the important properties quoted, thus leaving the manufacturer free to use any of the parts that are available for such a function. To cover the example the following is all that need be stated: 0.1µF 0402, say 16V, ceramic capacitor.

Newbury Electronics Ltd manages its own standard stock lists; all the designer needs to do is select an item from the standard stock list (train stock in NEL's case) and a wide range of components will become available. Follow the following link for instructions: http://www.newburyinnovation.co.uk/manufacturing/design-for-manufacture-dfm-electronic-component-selection/

4.11.2 FLYING PROBE DATA

This section relates to DfT (design for test). A flying probe test machine is one that places/connects a pin to a reference node on a PCBA, e.g. 0V, and then has another pin connect to other nodes in the circuit: the impedance between the two points is then measured and compared to the value, with a tolerance, which is expected between those two particular nodes. Flying probe testing can be more extensive since it is possible to have advanced machines stimulate circuits with signals and set up proper ATE (automatic test equipment) using products like Labview, which means that is possible to do extensive functional testing with flying probe testers.

KEY POINTS:

- ***Be aware that heavier components may fall off the PCB during assembly. Keeping heavier components on one side of the PCB can help with manufacture. The following is a general rule that aids with deciding whether or not components should be considered 'heavy'***
    - • 45mg/mm2 for SnAgCu solder
    - 60mg/mm2 for SnPb solder

- ***Use standard stock for all non-critical passive components (resistors and capacitors)***
- ***Consider including upper and lower values on all passive components listed in BoM. This may make the process of setting up basic flying probe testing quicker and/or cheaper.***

4.12 REFLOW OVEN/SOLDERING

There are a number of undirected soldering techniques, and the two are covered under this section.

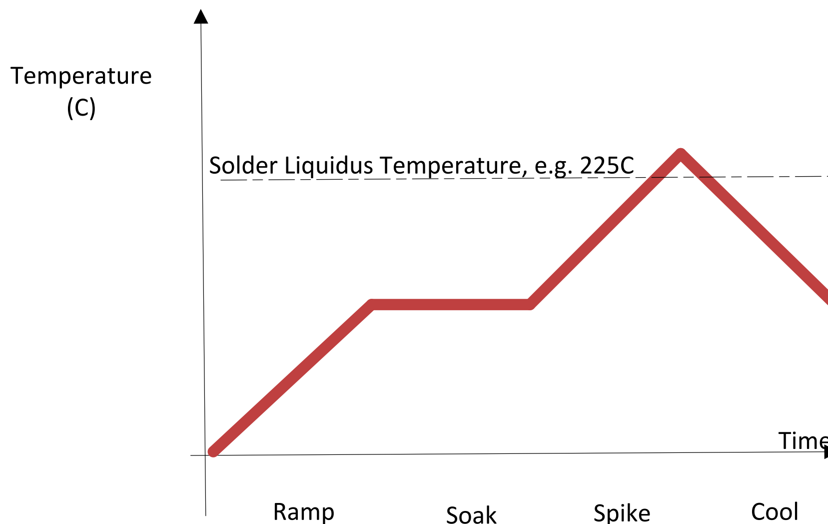
A PCB, having had solder paste applied and SMD components placed in the right positions, must then be heated to melt the solder and mechanically and electrically fix the components. Re-flow ovens are widely used for this purpose, and vapour phase soldering is ideal for doing soldering requirements that might challenge the re-flow technique.

(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)

As with all sections of this document it must be noted that the detail given is that which is considered suitable for a design engineer and not a production engineer. A production engineer will need to understand much more about the function of the machines involved.

A re-flow oven is simply an oven with heating zones that are finely controlled. The workpiece travels through these heated zones via a conveyor. A couple of points to note are that the zones are finely controlled with respect to each other, i.e. one zone should not affect the temperature of another (within reason); and that the design of such ovens is such that the ambient conditions outside the oven do not affect the zones.

A typical profile is shown below:



Re-flow soldering is subject to conflicting commercial and technical pressures. In order for the process to make money it must convey PCBAs at the maximum speed possible but a much slower speed would suit those wishing for the final product to be of the highest quality. What must be sought is the fastest speed possible commensurate with the necessary level of quality.

Put a description and drawing in here to illustrate why it may make sense to put heavy components on one side and lighter ones on the other.

Explain about Paste in Pin here – stencil PTH's and force paste into them, populate and then reflow.

KEY POINTS:

- ***The Ramp gradient must not be too great because the gaseous nature of the solder paste causes 'solder balls' to be spat over the PCB.***
- ***The Ramp gradient and resulting Soak phase must not be too slow because insufficiently heated solder forms a grape texture (known as graping)***
- ***The solder paste manufacturer's guidelines may be used but these will always be qualified by the performance of a particular oven and the characteristics of the PCBA in question. Generally speaking the Ramp is between 2 and 4C/s for the Ramp phase.***
- ***Sacrificial PCBAs may be used to find the right profile for a particular job***

(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)

- ***Thermally massive components should be distributed over the PCB, but note that this may have to be a trade off with EMC because partitioning of the PCBA may conflict with this requirement. A good designer will find a balance.***
- ***Try to place heavy components on one side of the PCBA and lighter ones on the other***
- ***Make sure an edge has been left on the PCBA such that the conveyor can grip the board***

4.13 VAPOUR PHASE SOLDERING

Vapour phase soldering involves holding PCBAs, that haven't been soldered but have been pasted and had SMD components placed, in a cloud of the vapour of a complex chemical. The vapour's temperature is above the liquidus temperature for the solder. The vapour condenses and in so doing melts the solder (note that the vapour is completely inert with respect to the PCBA's component parts). Very tight temperature control can be achieved with vapour phase soldering machines, and this makes them better suited to coping with PCBAs that don't have particularly good copper balance.

Vapour phase soldering is actually falling out of favour because the vapours are environmentally unfriendly and it is slow. Nevertheless such machines are good for dealing with thermal balance problems and low volume manufacture.

KEY POINTS:

- ***Don't target very large PCBAs at vapour phase soldering – there is a tendency for the vapour cloud to collapse if the quantity of soldering required is too great.***

4.14 MANUAL THROUGH HOLE SOLDERING

All the assembly machinery that has been described so far is used for SMD manufacture, but many designs still require some through-hole parts (connectors, heavy components, switches that require mechanical strength). This document will not cover the intricacies of hand soldering but there are some rules the designer should consider with regard to component placement and the connection of cabling.

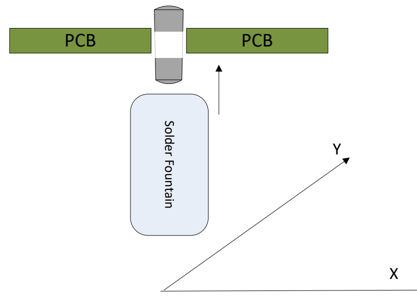
KEY POINTS:

- ***The quality of hand soldering is fully covered by the IPC 610 standard. Make sure that you specify the IPC standard required (IPC class I, II or III).***
- ***Pay special attention to the proximity of through hole components - it is all too easy to place parts in positions that it is impossible for a human to fit.***

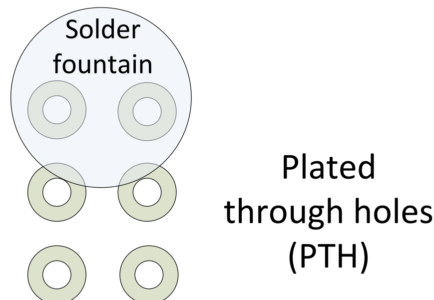
4.15 SELECTIVE SOLDERING

A selective soldering machine is one that carries out the function of through-hole soldering by creating a fountain of solder that is made to move to X-Y coordinates that correspond to pins that need to be soldered.

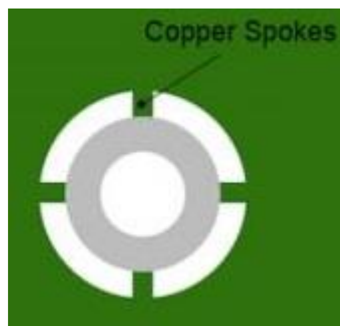
(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)



The main issue that arises is dwell time. The solder fountain is normally of considerably greater diameter than the pin that is being soldered, and as such may well cover a greater area than just the area that needs soldering. The fountain needs to dwell just long enough to make sure that a proper join is made but not long enough to risk a bridge. The diagram below illustrates this.



The main element of design that reflects on the performance of this machine is **thermal relief**.



Thermal relief, as in the diagram above, is applied when there is a significant quantity of copper attached to a PTH, as is the case with a plane. The problem is that the plane drains heat from the joint during soldering possibly resulting in faulty soldering. The spokes limit the flow of heat to the plane and allow the PTH to rise in temperature for good soldering. It is of course necessary to balance this with the increase in electrical resistance/impedance. This effect obviously has a profound effect on dwell times with selective soldering.

KEY POINTS:

- ***Production authorities will probably wish for thermal relief on virtually all PTHs that are attached to planes, but this must be balanced with the design specification. Thermal relief degrades the current rating and introduces increased impedance across itself that affects EMC performance. The engineer must balance the needs of the design against the demands of DfM.***

5. INSPECTION AND TEST

For a complete picture of the means by which a PCBA is reified it is essential to consider the kinds of inspection and test that apply to the process.

5.1 FLYING PROBE

Flying probe testing has already been covered earlier in this document

5.2 AOI

There are machines that use photographic images to monitor the quality of products. A high quality image is made of a PCBA that is known to be correct (gold standard), and then the AOI machine takes images of each example of production and compares them to the gold standard. This method will find all sorts of faults: incorrectly orientated chips; diodes the wrong way round; lifted pins; and many other issues, but it will find many false faults, e.g. nominal change in the marking on the top of a chip. The problem is that there is a possibility of the machine 'crying wolf' too often and operators consequently ignoring important issues. The most modern AOIs are 3D and this brings in assessment of solder joins as well as components.

KEY POINTS:

- ***Be clear whether or not your manufacturer has and uses AOIs. If carrying out an audit try to probe and find out how effectively the AOI facility is used.***
- ***Modern 3D AOIs collect statistics and lend themselves to advance quality assurance, e.g. six sigma. Assessing the existence of this is a good way measure the real quality of a supplier (one that does this is almost certainly from the top draw).***

5.3 X-RAY

The problem with some modern electronics is that it is impossible to visually inspect, e.g. BGAs and fillet penetration in PTHs, and it is to assist with this that X-ray machines find a use. A BGA, which is a microchip with its pins underneath it in the form of small balls, gives no visual access to the points at which it is soldered. The X-ray machine permits the quality of these joins to be assessed.

5.4 VISUAL TESTING

All manufacturers have magnification equipment and people whose job it is to find issues with PCBAs. This is laborious work and it really is much better if such work is covered by AOI and flying probe machines. It, nevertheless, remains a main feature of test and inspection with most British manufacturers that extensive visual inspection is done.

5.5 FUNCTIONAL TESTING

The greatest confidence that a PCBA has been correctly manufactured is given by a functional test (power put on the PCBA and it is made to carry out the functions for which it was designed). Despite this ultimate confidence the following are typical problems/advantages:

- It is expensive to design the necessary test jigs
- It is usually impractical to test every permutation and combination of function, and the test is consequently not entirely thorough.

- Flying probe testing can very thoroughly implement functional testing with no test jig overhead, or at most a very much reduced jig overhead.

- PCB layout
    - Partitioning
    - Grounding
    - Digital and Analogue circuit design
    - Interfaces
    - Filtering and shielding
    - Thermal relief (IPC 222A covers this)
    - Heat sinks and ventilation

- Mechanical Issues
    - Mechanical Fitting
    - Thickness of PCBs
    - 3D Views
    - Planes
    - Fiducials

- Design Tick List

- Testing

This will cover inspection standards (IPC –A-610), AOI machines, Flying probe testing, X ray machines and general inspection standards.

- Common Errors

A list of the most common errors found during manufacturing at Newbury Electronics Ltd.

(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)

6. GLOSSARY

BoM – bill of materials

CAD eye – the phenomenon whereby a designer, seeing everything clearly and magnified on a computer screen, designs something that is totally impractical on a real life scale, e.g. screen printing 0.1mm high.

CMRR – common mode rejetion ratio

Copper Balance – this means ensuring the spread of Cu over a layer is as even as possible. There should be no 'copper deserts'.

Copper Weight – the weight of copper if that thickness were plated over one square foot

Common mode noise – electromagnetically induced noise that stimulates both supply and return sides of an EUT such that noise currents in both the supply and return flow in the same direction

Differential mode noise – electromagnetically induced noise that stimulates current flow in around a loop formed by the signal carrying part of the circuit – not with reference to ground, noting that a notional zero volt connection on a PCBA may not actually be ground.

DfM – design for manufacture

DRC – design rule check (most CAD packages have them)

Earth – ultimate earth – terrestrial. Saftey earth.

EM – electromagnetic

EM waves – electromagnetic waves

EMC – electromagnetic compatibility

EMI – electromagnetic interference

ESD – electrostatic discharge

EUT – equipment under test

FEXT – far end crosstalk, usually quoted in dB

Ground – reference 0V

IC – integrated circuit

Microvias – vias with a diameter of less than 150µm (note some manufacturer's claim to be able to provide 15µm microvias

NEXT – near end cross talk, usually quoted in dB

Overlay - this is simply another word for silkscreen

PCB – printed circuit board

PCBA – assembled PCB (has components soldered to it)

(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)

PSU – power supply unit

PTH – plated through hole

SMD – surface mount device

Tenting – covering of a via with solder mask

Thermal relief – designing a PTH such that it is spoked. The reason is to increase the thermal resistance between a plane and an item that needs to be soldered, say a pin. This is done to make it possible to heat the pin enough for solder to flow (with a normal PTH this may be difficult without using a very hot soldering iron that damages the solder). Care must be taken to ensure that in increasing the thermal resistance the electrical resistance hasn't become compromised.

WDT – watchdog timer

7. REFERENCES

Tim Williams. *EMC for Product Designers* (Newnes 2010).

Printed Circuits Handbook (McGraw Hill Education 2016)

(Note use of the singular, masculine, possessive pronoun is deemed to cover both the masculine and the feminine)